E-BOOK

Best of Power Tips

A collection of insights from our power design experts

Introduction

In 2008, the power-management experts at Texas Instruments (TI) launched a series in EDN magazine called "Power Tips," focused on common tips and tricks of power-supply design. The articles address specific design challenges and provide flexibility for designers of power applications.

This e-book highlights the 25 most popular Power Tips articles from EDN.com. Although this e-book is not an exhaustive collection of all power challenges, it does address many of the more common and persistent problems designers face today, such as reaching lower quiescent current and increasing power density.

If you have questions about the topics covered here, submit them to the TI E2E™ design support forums Power Management forum.

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Technical Article

Make sure your optocoupler is properly biased

Brian King

In isolated power supplies, optocouplers pass the feedback signal across the isolation boundary. Optocouplers contain both a light-emitting diode (LED) and a photo detector. Current flowing through the LED results in a proportional current flowing in the photo detector. The current transfer ratio (CTR) is the current gain from the LED to the photo detector, and typically has a very wide tolerance. When you are designing an isolated feedback network, you must consider the tolerance of the optocoupler and all other components that determine the large signal gain. Neglecting this task could easily result in returns after your product goes to production.

The schematic for an isolated feedback network, shown in Figure 1, is the most common implementation. TI's TL431 contains both an error amplifier and reference. The resistor divider of R3 and R5 and the internal reference of the TL431 set the output voltage. The feedback network controls the power delivered to the power-supply output by varying the voltage on the feedback pin of the pulse-width modulation (PWM) controller. When V_{OUT} drifts higher, the TL431 cathode pulls more current through the optocoupler, which pulls the feedback pin lower. When V_{OUT} drifts lower, the TL431 cathode commands less current from the optocoupler, allowing the feedback pin to float higher.

A proper design must ensure that this circuit is capable of driving the feedback pin of the controller over its entire dynamic operating range while considering worst-case tolerances of all major variables.

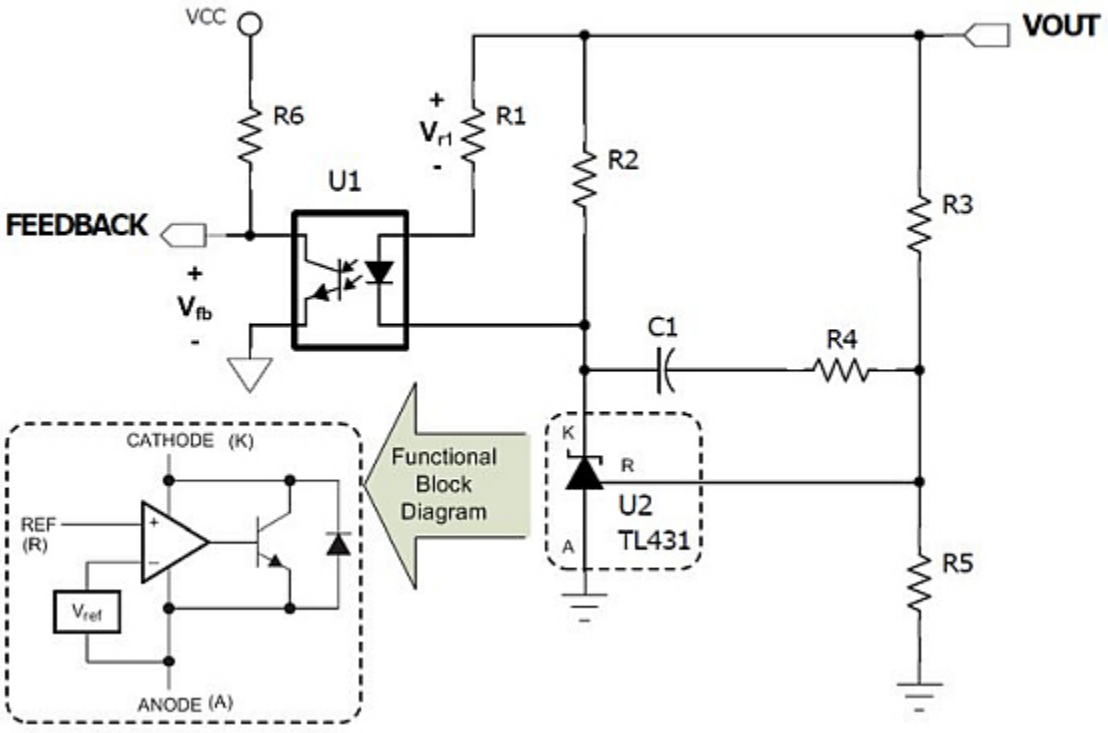

Figure 1. This circuit commonly generates the feedback signal in isolated power supplies.

The first step is to determine the dynamic operating range of the feedback pin in the controller. All controllers are different, so this task requires some investigation of the data sheet. As an example, let's assume that you are using an UCC2897A to control a 12V output active clamp-forward converter. Reading the "Detailed Pin Descriptions" in the UCC2897A data sheet reveals that a voltage of 2.5V on the feedback pin results in a zero duty cycle, while a feedback voltage of 4.5V results in a maximum duty cycle. The UCC2897A also provides a 5V reference, which you can use to bias the photo detector of the optocoupler through R6 in Figure 1. This reference has a minimum value of 4.75V and a maximum value of 5.25V. Equations 1 and 2 calculate the required current range through the optocoupler photo detector, assuming that you use a 1kΩ resistor with a 1% tolerance for R6:

$$I_{R6\_max} = \frac{V_{REFmax} - V_{FBmin}}{R_{6min}} = \frac{5.25V - 2.5V}{990\Omega} = 2.78mA \quad (1)$$

$$I_{R6\_min} = \frac{V_{REFmin} - V_{FBmax}}{R_{6max}} = \frac{4.75V - 4.5V}{1010\Omega} = 2.75mA \quad (2)$$

Your circuit must be able to drive the R6 current over a range of 0.25mA to 2.78mA. By providing resistor R2, the cathode of the TL431 is able to raise to a high-enough voltage, eliminating current flow in the optocoupler's LED. Thus, the circuit design guarantees the minimum R6 current, and you only need to worry about providing the maximum R6 current.

The second step is to calculate the worst-case CTR of the optocoupler. Optocouplers with "817" in the part number are offered from numerous manufacturers and are pin-for-pin compatible with each other; each uses a different prefix in the part number. Table 1 shows examples of 817 devices with different CTR ranges, denoted by a single-letter suffix in the part number. This CTR range does not include the effects of temperature and bias current. Charts from the optocoupler data sheet, recreated in Table 1 **and** Figure 3, summarize the effects of temperature and bias current.

Table 1. Optocouplers are available with various CTR ranges

Part No. suffix	CTR minimum	CTR maximum
A	80%	160%
B	130%	260%
C	200%	400%
D	300%	600%
None	80%	600%

Assume that you expect your supply to operate in a −40°C to 85°C environment. From , you know that you need to multiply the minimum CTR by a factor of about 0.7 at 85°C. If you select the "A" version of the 817, your minimum CRT can now be as low as 56%. Dividing the result of Equation 1 by 0.56 tells you that you may require at least 4.96mA of LED current, not including the effects of bias current. From, you can see that the bias-current effects at 4.96mA are negligible.

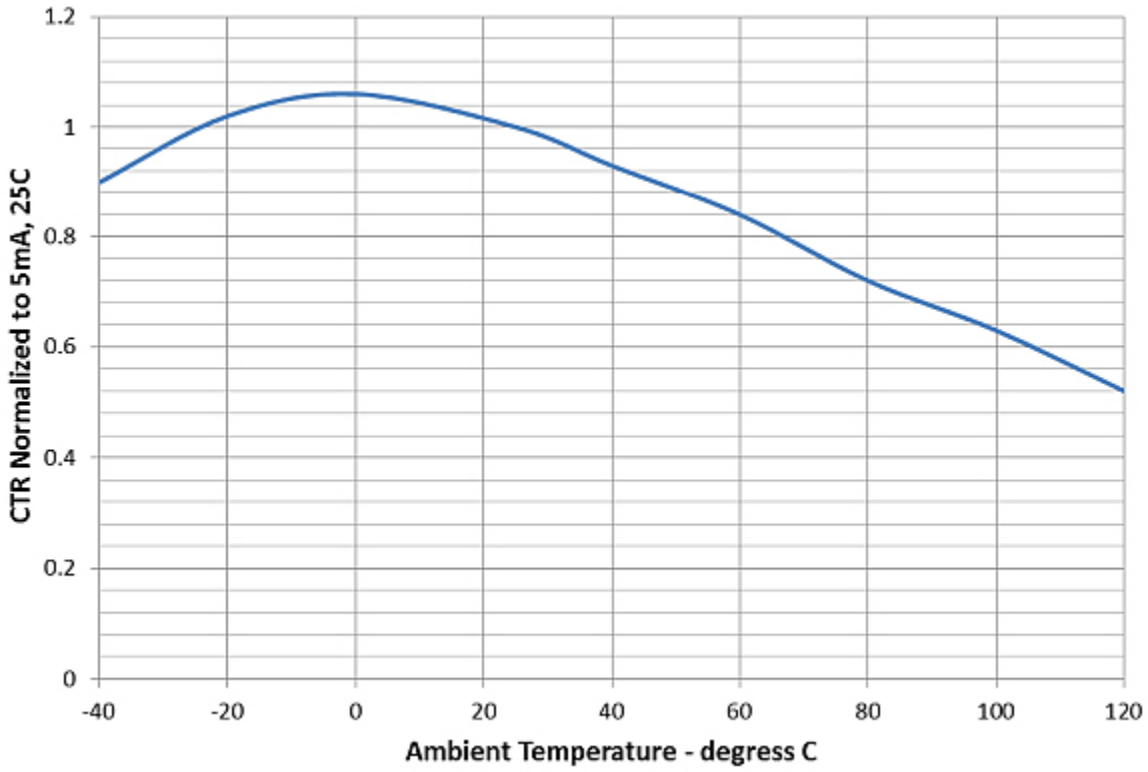

Figure 2. Optocoupler CTR varies with temperature.

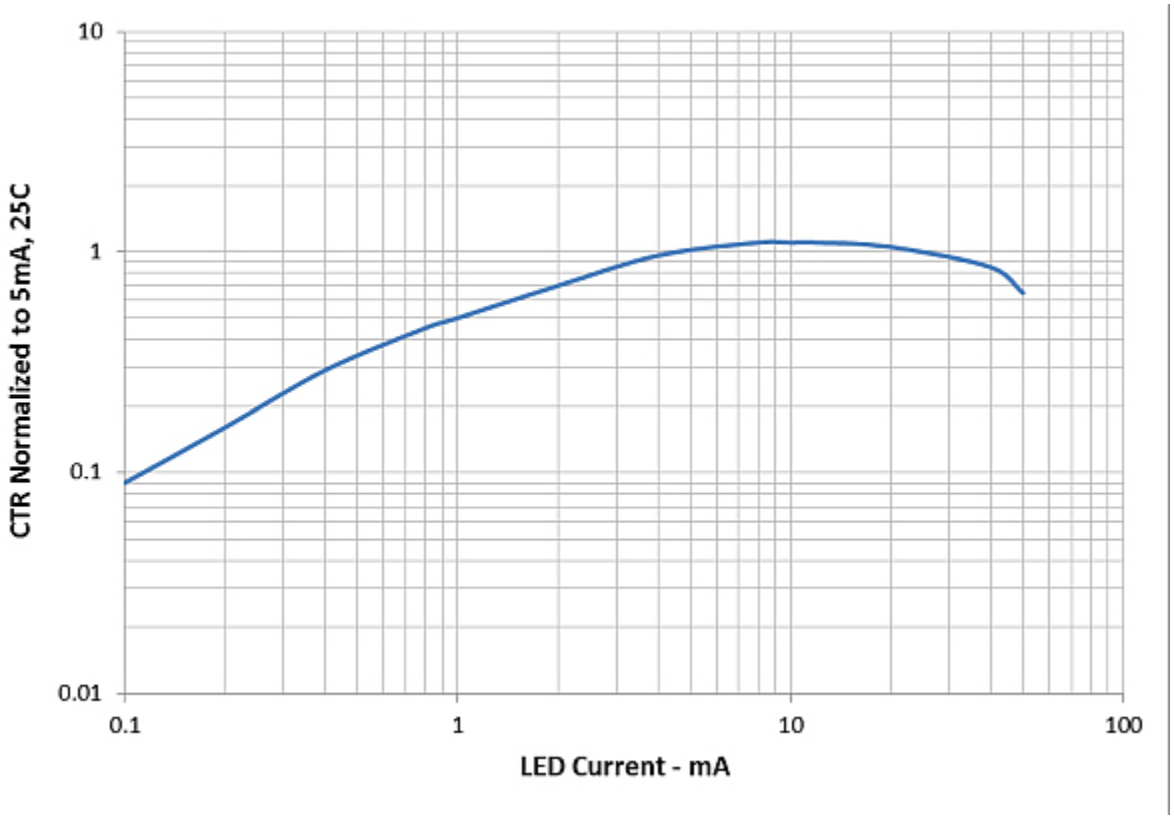

Figure 3. Optocoupler CTR varies with bias current.

The third and final step is to set the value of R1 to ensure that the TL431 can sufficiently drive the optocoupler over all conditions. The minimum cathode voltage of the TL431 is 2.5V, and the forward drop of the optocoupler's LED can be as high as 1.0V. Equation 3 calculates the maximum value of R1 to guarantee regulation:

$$R_{1max} = \frac{VOut - V_{TL431} - V_{LED}}{I_{R1min}} = \frac{12V - 2.5V - 1.0V}{5mA} = 1.7k\Omega \quad (3)$$

Using an R1 value greater than 1.7kΩ in this power supply may prevent the TL431 from driving enough current in the LED to maintain regulation. If the optocoupler is current-starved, the output voltage will keep rising until the proper amount of LED current conducts through the optocoupler. This results in overvoltage conditions on the output, and is more likely to occur at higher temperatures.

Tolerance issues such as this often slip through during the design phase. A pre-production run of power supplies could easily pass all tests, with the problem only showing up later as customer returns. Following the simple design procedure here can save your company money and keep your customers happy.

For more Power Tips, check out TI's Power Tips blog series on Power House.

Related articles

- Guidelines for reading an optocoupler datasheet
- Optocoupler simplifies power-line monitoring
- Power Tips #80: Compensating for diode drop variations

Technical Article

Designing a DCM flyback converter

John Betten

Flyback converters can operate either in continuous-conduction mode (CCM) or discontinuous-conduction mode (DCM). For many low-power and low-current applications, though, the DCM flyback converter can provide a more compact and lower-cost option. Here is a step-by-step methodology to guide you through such a design.

DCM operation is characterized by the converter having its rectifier current decreasing to zero before the start of the next switching cycle. Decreasing the current to zero before switching will reduce dissipation in the field-effect transistor (FET) and reduce rectifier losses, and will often reduce the transformer size requirement as well.

By comparison, CCM operation maintains rectifier current conduction through the end of the switching period. We covered flyback design trade-offs and power-stage equations for a CCM flyback in Power Tips #76: Flyback converter design considerations and Power Tips #77: Designing a CCM flyback converter. CCM operation is best suited for medium- to high-power applications, but if you have a low-power application that could use a DCM flyback, read on.

Figure 1 shows a simplified flyback schematic, which can operate in either DCM or CCM mode. Further, the circuit can switch between modes depending on timing. To maintain operation in DCM mode, which is what this article will evaluate, the key component switching waveforms should have the characteristics shown in Figure 2.

Operation starts when FET Q1 turns on for duty cycle period D. The current in T1's primary winding, which always starts at zero, reaches a peak set by the primary winding inductance, the input voltage, and on-time t1. During this FET on-time, diode D1 is reverse-biased because of T1's secondary winding polarity, forcing all output current to be supplied by output capacitor COUT during time periods t1 and t3.

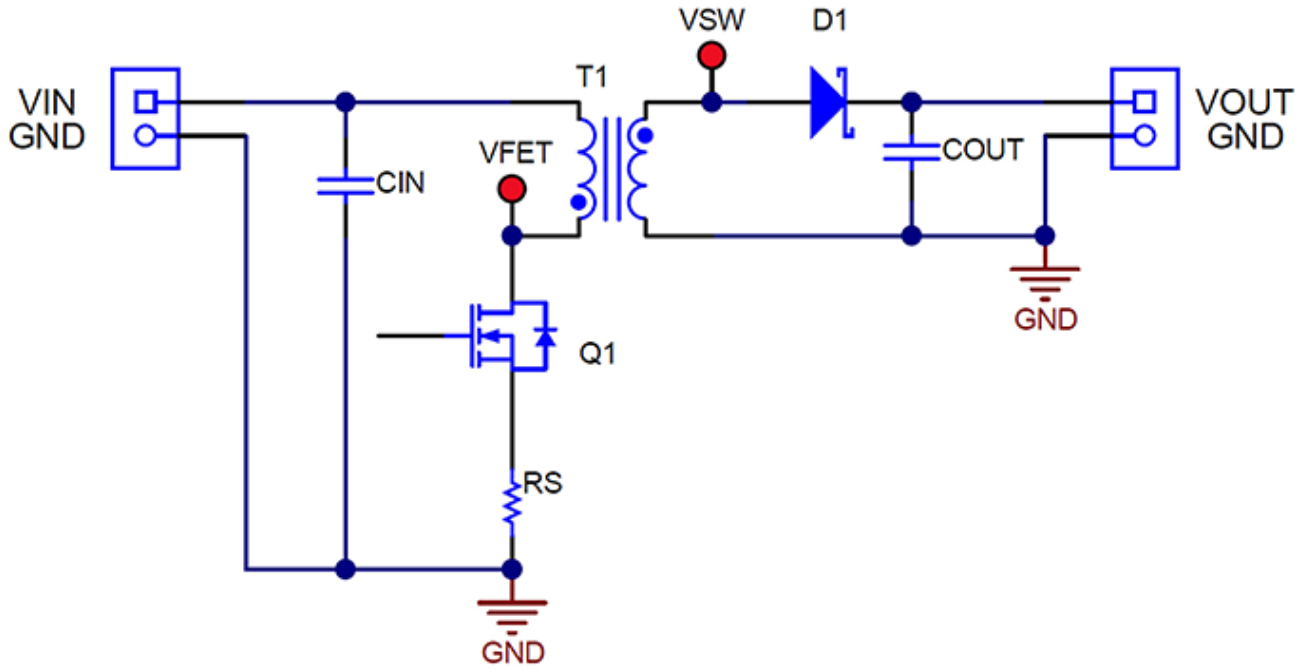

Figure 1. This simplified flyback converter can operate in either DCM or CCM.

When Q1 turns off during period 1-D, T1's secondary voltage polarity reverses, which allows D1 to conduct current to the load and recharge COUT. Current in D1 decreases linearly from its peak to zero during time t2. Once T1's stored energy is depleted, only residual ringing occurs during the remainder of period t3. This ringing is primarily due to T1's magnetizing inductance and to the parasitic capacitances of Q1, D1, and T1. This is easily seen in Q1's drain voltage during t3, which drops from VIN plus the reflected output voltage back to VIN, since T1 cannot support a voltage once current flow stops. (Note: Without an adequate dead time for t3, CCM operation may occur.) Currents in CIN and COUT are identical to those in Q1 and D1, but without a DC offset.

Shaded areas A and B in Figure 2 highlight the transformer's volt-microsecond products during t1 and t2, which must be in balance to prevent saturation. Area "A" represents (Vin/Nps) × t1 while "B" represents (Vout + Vd) × t2, both referenced to the secondary side. Np/Ns is the transformer primary-to-secondary turns ratio.

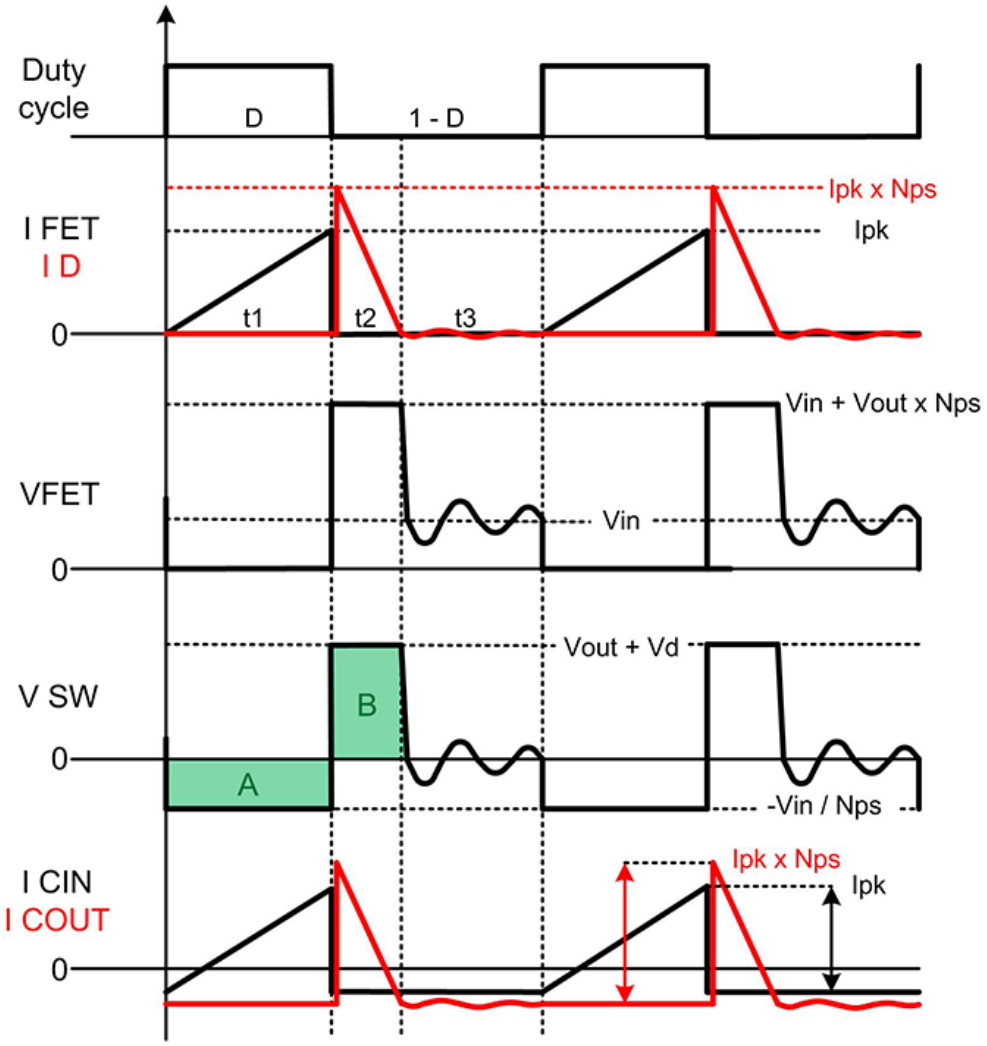

Figure 2. The key voltage and current switching waveforms for a DCM flyback include several critical parameters that designers must specify.

Table 1 details characteristics of DCM operation relative to CCM. One key DCM attribute is that having a lower primary inductance decreases the duty cycle, regardless of the transformer's turns ratio. This attribute lets you constrain your design's maximum duty cycle. This can be important if you are trying to use a specific controller or stay within certain on or off time limits. A lower inductance, which requires a lower average energy storage (albeit with a higher peak FET current), also often results in allowing a smaller transformer than a CCM design would require.

Another DCM advantage is that the design eliminates D1 reverse-recovery losses in standard rectifiers, since the current is zero at the end of t2. Reverse-recovery losses often appear as increased dissipation in Q1, so eliminating them reduces stresses on the switching transistor. The benefit of this becomes increasingly important at higher output voltages, where the reverse-recovery times of rectifiers increase with higher-voltage-rated diodes.

Table 1. DCM flyback designs have both advantages and drawbacks relative to CCM designs.

DCM advantages	DCM disadvantages
Lower primary inductance than CCM	Higher peak primary current
Inductance sets the maximum duty cycle	Higher peak rectifier current
Smaller transformer possible	Increased input capacitance
No rectifier reverse-recovery losses	Increased output capacitance
No (or minimal) FET turn-on losses	Potentially increased electromagnetic interference
No right half-plane zero in the control loop	Wider duty-cycle operation than CCM
Optimal for low output power	Increased bandwidth variation

Developers will need to know several key parameters when starting a design, along with the basic electrical specification. Begin by selecting a switching frequency (f_{sw}), a maximum desired operating duty cycle (D_{max}), and an estimated target efficiency. Equation 1 then calculates on time t1 as:

$$t1 = \frac{Dmax}{fsw} \tag{1}$$

Next, estimate the transformer's peak primary current, Ipk, using Equation 2. For the FET's on voltage (Vds_on) and the current-sense resistor voltage (VRS) in Equation 2, assume small voltage drops that are appropriate for your design, like 0.5 V. You can update these voltage drops later.

$$Ipk = \frac{Pout_{max} \times \left(\frac{2}{D_{max}}\right)}{(Vin_{min} - Vds\_on - VRS) \times (n)} \tag{2}$$

Equation 3 calculates the required transformer turns ratio, Np/Ns, based on equating areas A and B in Figure 2:

$$\frac{Np}{Ns} = \frac{(Vin_{min} - Vds\_on - VRS) \times t1}{\left(\frac{1}{fsw} \times (1 - x) - t1\right) \times (Vout + Vd)} \tag{3}$$

where x is a desired minimum idle time for t3 (starting with x = 0.2).

If you would like to change Np/Ns, adjust D_{max} and iterate again.

Next, calculate the maximum "flat-top" voltages for Q1 (Vds_max) and D1 (VPIV_max) using Equation 4 and Equation 5:

$$Vds_{max} = Vin_{max} + (Vout + Vd) \times \frac{Np}{Ns} \tag{4}$$

$$VPIV\_max = Vout + \frac{Vin\_max}{\frac{Np}{Ns}} \tag{5}$$

Since these components generally have ringing due to transformer leakage inductance, a rule of thumb is to expect the actual values to be 10-30% higher than Equation 4 and Equation 5 predict. If Vds_max is higher than anticipated, reducing D_{max} will lower it, but VPIV_max will increase. Determine which component voltage is the more critical and iterate again if necessary.

Calculate t1_max using Equation 6, which should be close to that in Equation 1:

$$t1\_max = \frac{(Vout + Vd) \times \frac{Np}{Ns} \times \left(\frac{1}{fsw} \times (1 - x)\right)}{Vin_{min} + (Vout + Vd) \times \frac{Np}{Ns}} \quad (6)$$

Calculate the maximum required primary inductance with Equation 7:

$$Lpri\_max = \frac{Vin\_min^2 \times t1\_max^2 \times n \times fsw}{2 \times Vout \times Iout\_max} \quad (7)$$

If you select a lower inductance than Equation 7 indicates, increase x and decrease D_{max} until Np/Ns and Lpri_max are equal to your desired values by iterating as necessary.

You can now calculate D_{max} in Equation 7:

$$Dmax = \sqrt{\frac{2 \times fsw \times Vout \times Iout\_max \times Lpri}{Vin\_min^2 \times n}} \quad (8)$$

And calculate the maximum Ipk and its maximum root-mean-square (RMS) value using Equation 9 and Equation 10, respectively:

$$Ipkmax = \sqrt{\frac{2 \times Vout \times Iout\_max}{Lpri \times fsw \times n}} \quad (9)$$

$$Ipkrms = Ipkmax\sqrt{\frac{Dmax}{3}} \quad (10)$$

Calculate the maximum current-sense resistor value allowed, based on the selected controller's current-sense input minimum current limit threshold, Vcs (Equation 11):

$$Rsmax = \frac{Vcs}{Ipkmax} \quad (11)$$

Use the values calculated for Ipkmax in Equation 11 and RS to verify that the assumed voltage drops for the FET Vds and sense resistor VRS in Equation 2 are close; iterate again if significantly different.

Use Equation 12 and Equation 13 to calculate the maximum power dissipated in RS and conduction losses in Q1 from Equation 10:

$$P\,Rsns = Ipkrms^2 \times RS \quad (12)$$

$$P\,FETcond = Ipkrms^2 \times Rdson \quad (13)$$

FET switching losses are generally highest at Vinmax, so it's best to calculate Q1 switching losses over the full range of VIN using Equation 14:

$$P\,FETsw = 0.25 \times \left(\frac{Qdrv}{Idrv}\right) \times fsw \times Ipk \times Vds \quad (14)$$

where Qdrv is the FET total gate charge and Idrv is the expected peak gate-drive current.

Equation 15 and Equation 16 calculate the total power loss from charging and discharging the FET's nonlinear Coss capacitance. The integrand in Equation 15 should closely match the actual FET's Coss data-sheet curve between 0 V and its actual operating Vds. Coss losses are generally greatest in high-voltage applications or when using very low RDS(on) FETs, which have larger Coss values.

$$Qtot = \int_{-Vds}^{0} \left[\frac{Coss\,(0V)}{(1 - v)^{0.5}}\right] dv \quad (15)$$

$$P\,FETcoss = \frac{fsw \times Qtot \times Vds}{2} \quad (16)$$

Total FET losses can be approximated by summing the results of Equation 13, Equation 14, and Equation 16.

Equation 17 reveals that the diode losses in this design will greatly simplify. Be sure to select a diode rated for the secondary peak current, which is generally much greater than IOUT.

$$P\,Diode = \frac{Ipk \times \frac{Np}{Ns} \times t2 \times fsw}{2} \times Vdiode = Iout \times Vdiode \quad (17)$$

Output capacitance is generally selected as the larger of Equation 18 or Equation 19, which calculate capacitance based on ripple voltage and equivalent series resistance (Equation 18) or load transient response (Equation 19):

$$Cout1\,ripple = \frac{Iout\_max \times (1 - D)}{\left(Vout\,rip - Ipk \times \frac{Np}{Ns} \times Resr\right) \times fsw} \quad (18)$$

$$Cout2\,Itran = \frac{\Delta Iout}{2\pi \times \Delta Vout \times fBW} \quad (19)$$

where ΔIOUT is a change in output load current, ΔVOUT is the allowable output-voltage excursion and fBW is the estimated converter bandwidth.

Equation 20 calculates the output capacitor RMS current as:

$$ICout\,rms = \sqrt{\frac{Ipk \times \left(\frac{Np}{Ns}\right)^2 \times t2 \times fsw}{3} - Iout\_max^2} \quad (20)$$

Equation 21 and Equation 22 estimate the input capacitor's parameters as:

$$Cinmin = \frac{Ipk \times D}{2 \times fsw \times Vin\,rip} \quad (21)$$

$$ICin\,rms = \sqrt{\frac{Ipk^2 \times D}{3} - \left(\frac{Pout\_max}{Vin \times n}\right)^2} \quad (22)$$

Equation 23, Equation 24, and Equation 25 summarize the three key waveform time intervals and their relationship:

$$t1 = \sqrt{\frac{2 \times Vout \times Iout \times Lpri}{Vin^2 \times fsw \times n}} \quad (23)$$

$$t2 = \frac{t1 \times Vin}{(Vout + Vd) \times \frac{Np}{Ns}} \quad (24)$$

$$t3 = \frac{1}{fsw} - t1 - t2 \quad (25)$$

If you need additional secondary windings, Equation 26 easily calculates additional winding, Ns2:

$$\frac{Ns2}{Ns1} = \frac{Vout2 + Vd2}{Vout1 + Vd1} \quad (26)$$

where VOUT1 and Ns1 are the regulated output voltage.

The transformer primary RMS current is the same as the FET RMS current in Equation 10; the transformer secondary RMS current is shown in Equation 27. The transformer core must be capable of handling Ipk without saturating. You should consider core losses too, but that is beyond the scope of this article.

$$Isec = Ipk \times \frac{Np}{Ns}\sqrt{\frac{t2 \times fsw}{3}} \quad (27)$$

As can be seen in the steps provided, the design of a DCM flyback is an iterative process. Some of your initial assumptions, such as switching frequency, inductance, or turn ratios, may change based on later calculations, like power dissipations. But remain diligent and go through the design steps as often as required to achieve the design parameters you need. An optimized DCM flyback design can provide a low-power, compact, and low-cost solution to power converter needs if you are willing to put in the effort.

Related articles

- Power Tips #76: Flyback converter design considerations
- Power Tips #77: Designing a CCM flyback converter
- Power Tips #87: How to design a high-voltage DCM inverting charge pump converter
- How to design a flyback converter as a front-end for a two-stage LED driver
- Implementing power factor correction with frequency clamp critical conduction mode
- Discontinuous conduction brings issues to current-mode converters

Technical Article

Designing a CCM flyback converter

John Betten

A continuous-conduction mode (CCM) flyback converter is often used in medium power, isolated applications. CCM operation is characterized by lower peak switching currents, less input and output capacitance, reduced EMI, and a narrower operational duty-cycle range than discontinuous-conduction-mode (DCM) operation. These virtues, along with being low cost, mean they have been widely adopted in commercial and industrial applications. This article will provide the power-stage design equations for a 53Vdc to 12V at 5A CCM flyback previously discussed in Power Tips: Flyback converter design considerations.

Figure 1 shows a detailed 60W flyback schematic, operating at 250 kHz. The duty-cycle is selected to be 50% maximum at the minimum input voltage of 51V and maximum load. Although operation beyond 50% is acceptable, it is not necessary in this design. The duty cycle will decrease only a few percent while in CCM operation because of the relatively low high-line input voltage of 57V. However, if the load is greatly reduced and the converter enters DCM operation, duty cycle will significantly decrease.

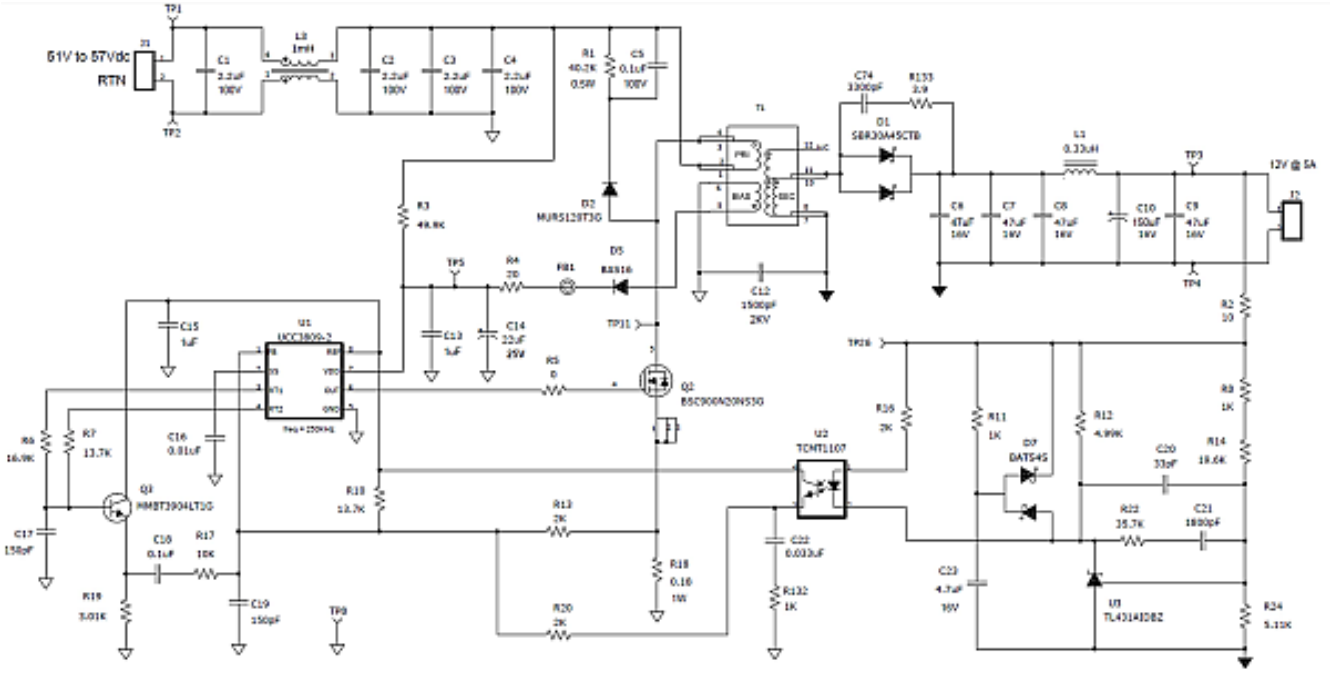

Figure 1. 60W CCM flyback converter schematic.

Design specifics

To prevent core saturation, the volt-second product for the windings on/off times must balance. This equates to Equation 1:

$$Vinmin \times dmax = (Vout + Vd) \times (1 - dmax) \times Nps, \; where \; NPS = \frac{Npri}{Nsec} \quad (1)$$

Set dmax to 0.5 and calculate the turn ratios for Nps12 (Npri : N12V) and Nps14 (Npri : N14V) as expressed by Equation 2 and Equation 3:

$$Nps12 = \frac{Vinmin}{(Vout + Vd)} \times \frac{dmax}{(1 - dmax)} = \frac{51V}{(12V + 0.5V)} \times \frac{0.5}{(1 - 0.5)} \sim 4\ (4{:}1\ step - down) \quad (2)$$

$$Nps14 = \frac{Vinmin}{(Vout + Vd)} \times \frac{dmax}{(1 - dmax)} = \frac{51V}{(14V + 0.5V)} \times \frac{0.5}{(1 - 0.5)} \sim 3.5\ (3{:}5{:}1\ step - down) \quad (3)$$

The operating duty-cycle and FET voltage can be calculated now that the transformer turns ratio is set (Equation 4 and Equation 5).

$$d = \frac{Nps12 \times (Vout + Vd)}{Vin + Nps12\,(Vout + Vd)} \times \frac{4 \times (12V + 0.5V)}{57V + 4 \times (12V + 0.5V)} \sim 0.47\ (dmin\ at\ Vin = 57V) \quad (4)$$

$$Vdsmax = Vinmax + Nps12 \times (Vout + Vd) = 57V + 4 \times (12V + 0.5V) = 107V \quad (5)$$

Vdsmax represents the “flat top” voltage on FET Q2 drain without ringing. Ringing is typically related to the transformer leakage inductance, parasitic capacitances (T1, Q1, D1), and switching speed. Derate the FET voltage an additional 25-50%, selecting a 200V FET. The transformer must have excellent coupling between windings and a maximum leakage inductance of one percent or less, if possible, to minimize ringing.

When Q2 is on, diode D1 has a reverse voltage stress equal to Equation 6:

$$VD1piv = Vout + \frac{Vinmax}{Nps12} = 12V + \left(\frac{57V}{4}\right) \sim 26V \quad (6)$$

Ringing is common when the secondary winding swings negative due to leakage inductance, diode capacitance and reverse recovery characteristics. See Equation 7.

$$ID1 = \frac{Ioutmax}{(1 - dmax)} = \frac{5A}{(1 - 0.5)} = 10A \quad (7)$$

I selected a 30A/45V rated D²PAK package to reduce the forward voltage drop to 0.33V at 10A. Power dissipation is equal to Equation 8:

$$PD1 = Ioutmax \times Vd = 5A \times 0.33V \sim 1.7W \quad (8)$$

A heat sink or airflow for proper thermal management is recommended. You can calculate the primary inductance from Equation 9:

$$Lmin = \frac{Vinmin^2 \times dmax^2 \times n}{2 \times fsw \times Poutmin} = \frac{51V^2 \times 0.5^2 \times 0.91}{2 \times 250KHz \times 15W} \sim 80uH \quad (9)$$

P_{OUTMIN} is where the converter enters DCM, which is typically 20-30% of P_{OUTMAX} .

Peak primary current occurs at V_{INMIN} and is equal to:

$$Ipri_{pk} = \frac{Ioutmax}{(1 - dmax) \times Nps12} + \frac{Vinmin \times dmax}{2 \times Lpri \times fsw} = \frac{5A}{(1 - 0.5) \times 4} + \frac{51V \times 0.5}{2 \times 80uH \times 250KHz} \sim 3.14A \quad (10)$$

This is necessary to determine the maximum current sense resistor (R18) value to prevent tripping of the controller’s primary over current (OC) protection. For the UCC3809, the voltage across R18 cannot exceed 0.9V to guarantee full output power. For this example, I choose a 0.18 Ohm value. A smaller resistance is acceptable as it reduces power loss. But too small a resistance increases noise sensitivity and makes the OC threshold high, risking transformer saturation or even worse, stress-related circuit failure during an OC fault. The power dissipated in the current sense resistor is Equation 11:

$$PRs = \left[\frac{Ioutmax \times \sqrt{dmax}}{(1 - dmax) \times Nps12}\right]^2 \times Rs = \left[\frac{5A \times \sqrt{0.5}}{(1 - 0.5) \times 4}\right]^2 \times 0.18\Omega \sim 0.56\text{W} \quad (11)$$

With calculated FET conduction and turn off switching losses are estimated from Equation 12 and Equation 13:

$$Pcond = \left[\frac{Ioutmax \times \sqrt{d}}{(1 - d) \times Nps12}\right]^2 \times Rs = \left[\frac{5A \times \sqrt{0.47}}{(1 - 0.47) \times 4}\right]^2 \times 0.12\Omega \sim 0.3\text{W}\ \ (Vin = 57V) \quad (12)$$

$$Psw = \frac{1}{4} \times tsw \times fsw \times Vds \times Ipri_{pk} = \frac{1}{4} \times 25nS \times 250KHz \times 160V \times 3.03A \sim 0.76W \quad (13)$$

Loss calculations associated with Coss are somewhat nebulous, as this capacitance is quite non linear, decreasing with higher Vds, and for this design is estimated to be 0.2W.

Capacitor requirements generally consist of calculating the maximum RMS current, the minimum capacitance necessary to obtain the desired ripple voltage and holdup for transients. Output capacitance and I_{OUTRMS} are calculated as Equation 14 and Equation 15:

$$Coutmin = \frac{Ioutmax \times dmax}{fsw \times Vripout} = \frac{5A \times 0.5}{250KHz \times 0.12V} = 83uF \quad (14)$$

$$Ioutrms = Ioutmax \times \sqrt{\frac{dmax}{1 - dmax}} = 5A \times \sqrt{\frac{0.5}{1 - 0.5}} = 5A \quad (15)$$

Ceramic capacitors alone are suitable, but seven would be required to realize 83 µF after DC-biasing effects. Therefore, I only chose enough to handle the RMS current and followed with an inductor-capacitor filter to reduce the output ripple voltage, as well as improve load transients. If large load transients exist, additional output capacitance may be required to reduce voltage droop.

The input capacitance is equal to Equation 16:

$$Cinmin = \frac{Ipri_{pk} \times dmax}{2 \times fsw \times Vinrip} = \frac{3.14A \times 0.5}{2 \times 250KHz \times 1.5V} = 2uF \quad (16)$$

Again, you must consider the capacitance-robbing DC-bias effect. As expressed by Equation 17 RMS current is approximately:

$$Iinrms = \frac{Ioutmax}{Nps} \times \sqrt{\frac{dmax}{1 - dmax}} = \frac{5A}{4} \times \sqrt{\frac{0.5}{1 - 0.5}} = 1.25A \quad (17)$$

Figure 2 shows the prototype converter's efficiency, while Figure 3 shows the flyback evaluation board.

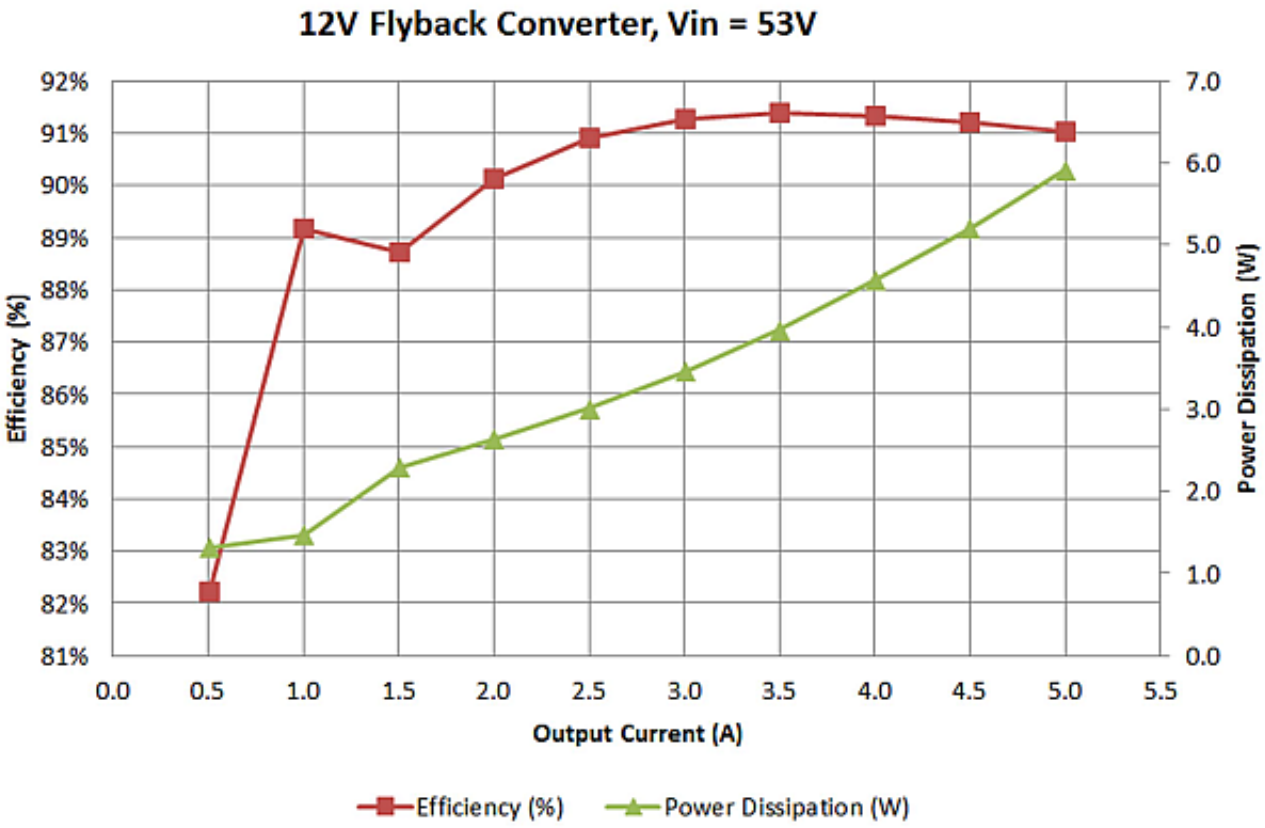

Figure 2. Converter efficiency and losses dictate package selection and thermal requirements.

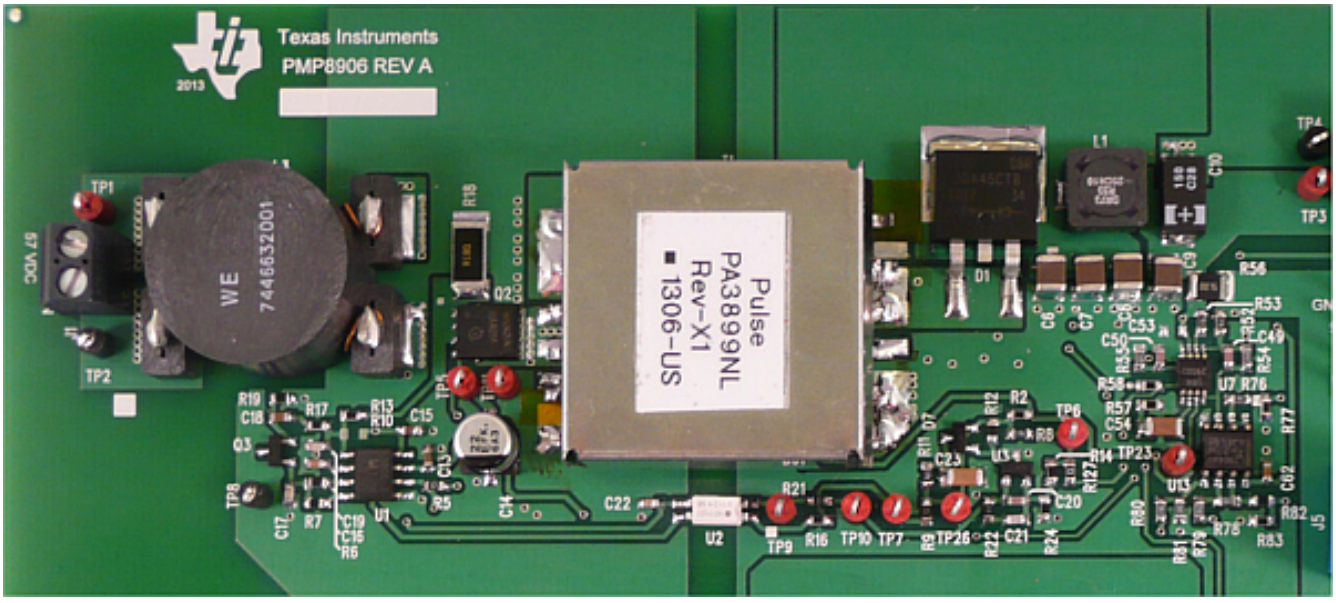

Figure 3. 60W flyback evaluation hardware measures 100mm by 35mm.

Aid in selecting the proper compensation component values can be investigated here: Compensating isolated power supplies.

This design example covers basic component calculations of a functional CCM flyback design. However, initial estimates often make it necessary to iterate the calculations in order to fine tune it. Still, more detail work is often necessary in areas such as transformer design and control-loop stabilization in order to obtain a well-working, optimized flyback.

Check out TI's Power Tips blog series on Power House.

Also see:

- Power Tips #76: Flyback converter design considerations
- Quasiresonant flyback converter easily charges energy-storage capacitors
- How to design a flyback converter as a front-end for a two-stage LED driver
- HV flyback converter improves efficiency

Technical Article

Flyback converter design considerations

John Betten

The many virtues of flyback converters include being the lowest-cost isolated power converter, easily supplying multiple output voltages, a simple primary-side controller and power delivery of up to 300W. Flyback converters are used in many offline applications from televisions to phone chargers as well telecommunications and industrial applications. Their basic operation can appear intimidating and the design choices are many, especially for those who have not designed one before. Let's look at some of the key design considerations for a 53 VDC to 12V at 5A continuous-conduction mode (CCM) flyback.

Figure 1 shows a detailed 60W flyback schematic, operating at 250 kHz. When FET Q2 turns on, the input voltage is applied across the transformer's primary winding. Current in the winding now ramps up, allowing energy to be stored in the transformer. Since output rectifier D1 is reverse-biased, current flow to the output is blocked. When Q2 turns off, primary current is interrupted, forcing the winding's voltage polarities to reverse. Current now flows out of the secondary winding, reversing the polarity of the winding voltage with the dot-voltage positive. D1 conducts, delivering current to the output load and recharging the output capacitors.

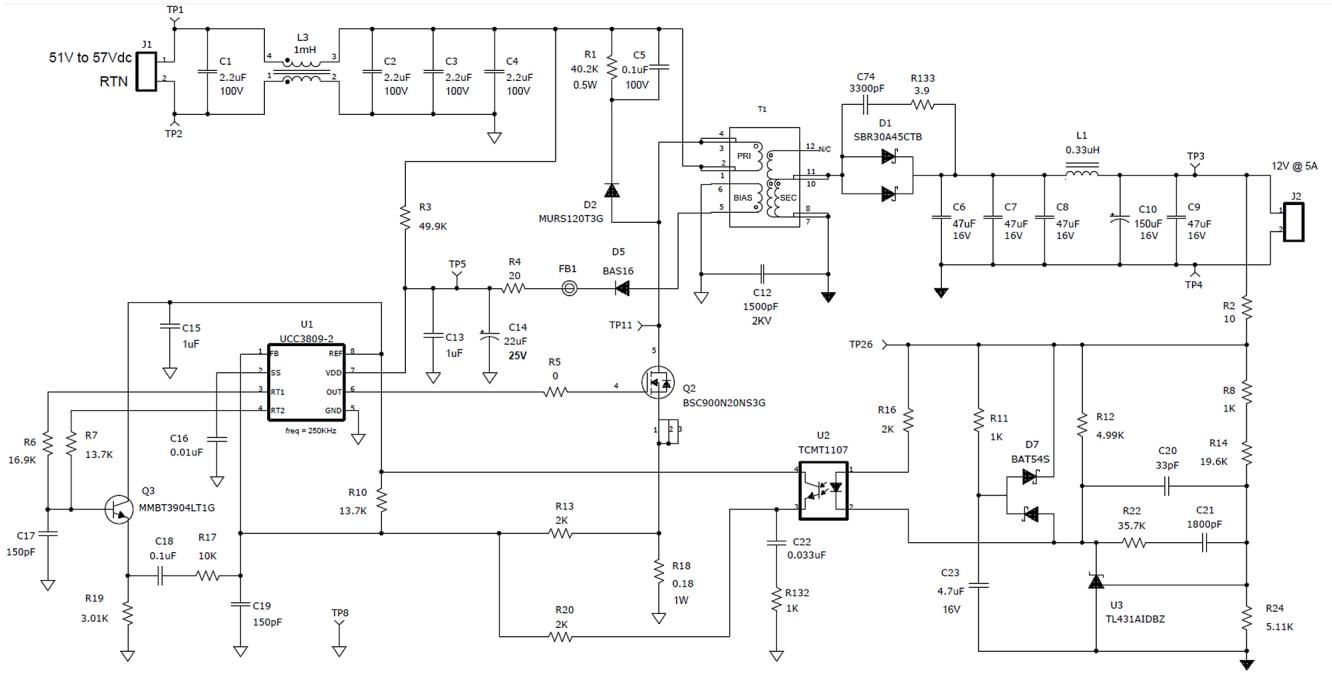

Figure 1. 60 W CCM flyback converter schematic.

Additional transformer windings can be added, or even stacked on top of other windings, to obtain additional outputs. However, the more outputs added, the worse their regulation will be. This because of the imperfect magnetic flux linkages between the windings and the core (coupling) and the physical separation of the windings, creating leakage inductance. Leakage inductance acts as stray inductance in series with the primary and the output windings. This creates an unintended voltage drop in series with the windings, effectively decreasing output voltage regulation accuracy. A general rule of thumb is to expect non-regulated outputs to vary +/–5 to 10%, over cross-loading, with a properly wound transformer. Additionally, a heavy-loaded regulated output can cause a large increase in an unloaded secondary output's voltage by peak-detecting leakage-induced voltage spikes. In this case, a preload or soft clamp can help limit the voltage.

CCM and discontinuous-conduction mode (DCM) operation each have their own merits. By definition, DCM operation occurs when the output rectifier current decreases to 0A before the next cycle starts. DCM operation benefits include a lower primary inductance typically resulting in a smaller power transformer, elimination of the rectifier's reverse-recovery losses and FET turn on losses, and no right-half-plane-zero. However, these advantages are offset by higher peak currents in the primary and secondary, increased input and output capacitances, increased electromagnetic interference (EMI), and decreased duty-cycle operation at light-load compared to CCM.

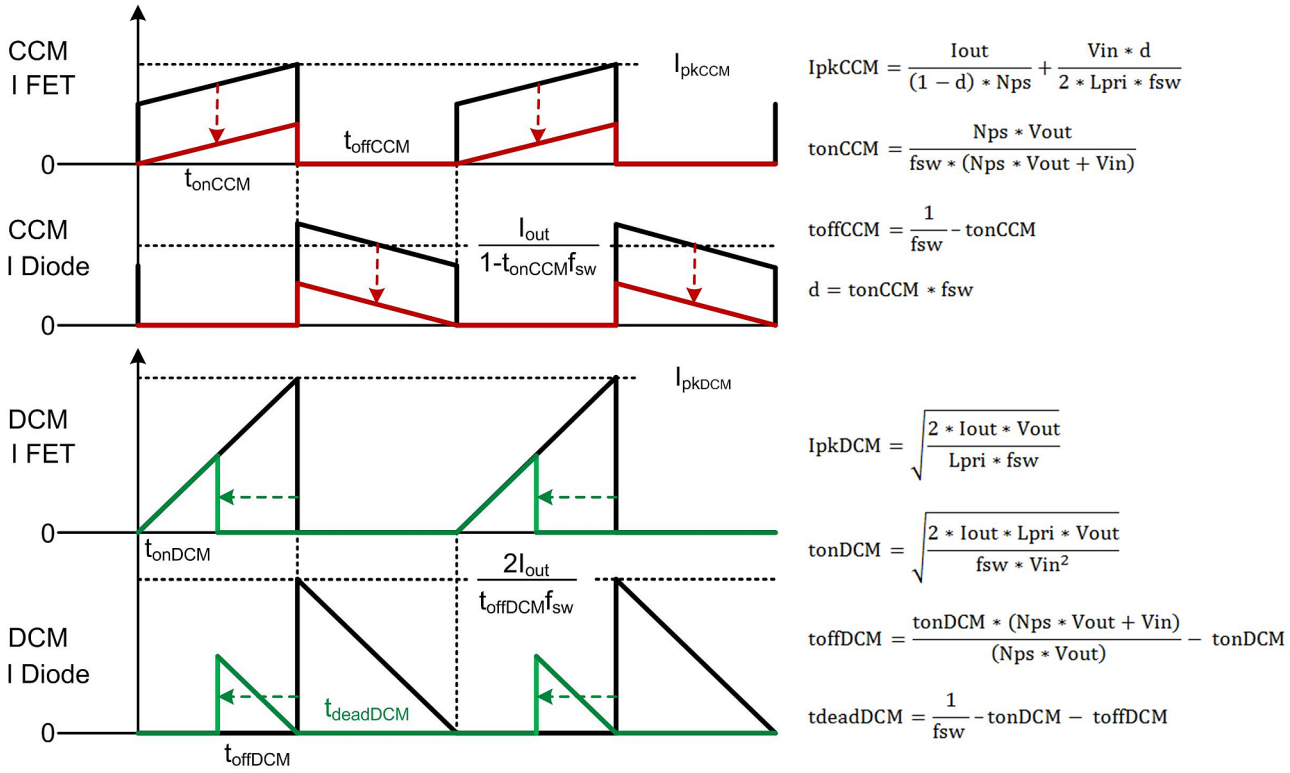

Figure 2. Comparison of CCM and DCM flyback FET and rectifier currents,

Figure 2 illustrates how currents in Q2 and D1 change while at minimum V_{IN}, and the load decreases from the maximum to ~25% in both CCM and DCM. In CCM, the duty cycle is constant for a fixed-input voltage and when the load is between its maximum and minimum design level (~25%). The current "pedestal" levels decrease with reduced loading until DCM is reached, at which point the duty-cycle decreases. In DCM, maximum duty-cycle only occurs at minimum V_{IN} and maximum load. The duty cycle decreases for increased input voltage or reduced load.

This can make the duty-cycle small at high-line and minimum load, so be sure your controller can operate properly at this minimum on-time. DCM operation introduces a dead-time for duty cycles below 50% after the rectifier current reaches 0A. It's characterized by a sinusoidal voltage on the FET drain and set by residual current, parasitic capacitances, and leakage inductance, but is generally benign. For this design, CCM operation was chosen because higher efficiency can be achieved from reduced switching and transformer losses.

This design uses a primary referenced 14V bias winding to power the controller after the 12V output reaches regulation, reducing losses versus being directly powered from the input. I chose a two-stage output filter for low-ripple voltage. The first-stage ceramic capacitors handle the high RMS current from the pulsating currents in D1. Their ripple voltage is reduced by filter L1 and C9/C10, providing about 10 times the ripple reduction along with reduced RMS currents in C9/C10. If a higher output ripple voltage is acceptable, the inductor-capacitor filter can be eliminated, but the output capacitors must be capable of handling the full RMS current.

The UCC3809-1 or UCC3809-2 controller is designed to interface directly with the U2 optocoupler for an isolated application. In non-isolation designs, U2 and U3 can be eliminated along with the voltage-feedback resistor-divider connected directly to a controller, such as the UCC3813-x series with internal error amplifier.

Switching voltages on Q2 and D1 create high-frequency common-mode currents in the transformer interwinding and component parasitic capacitances. Without the EMI capacitor C12 providing a return path, these currents would flow into the input and/or output, increasing noise or possibly erratic operation.

The combination of Q3/R19/C18/R17 provides slope-compensation by summing the oscillator's voltage-ramp into the primary current-sense voltage of R18, which is used for current-mode control. Slope-compensation eliminates sub-harmonic oscillation, a phenomena characterized by a wide duty-cycle pulse followed by a narrow one. Since this converter is designed to not exceed 50% operation, instead I added slope compensation to reduce switch-jitter susceptibility. However, excessive voltage-slope can push the control loop towards voltage-mode control and possible instability. Finally, the optocoupler transfers the error-signal from the secondary-side to keep the output voltage regulated. The feedback (FB) signal comprises the current-ramp, slope-compensation, output error signal, and DC offset to reduce the over-current threshold.

Figure 3 shows the voltage waveforms for Q2 and D1, displaying some leakage inductance and diode reverse-recovery induced ringing.

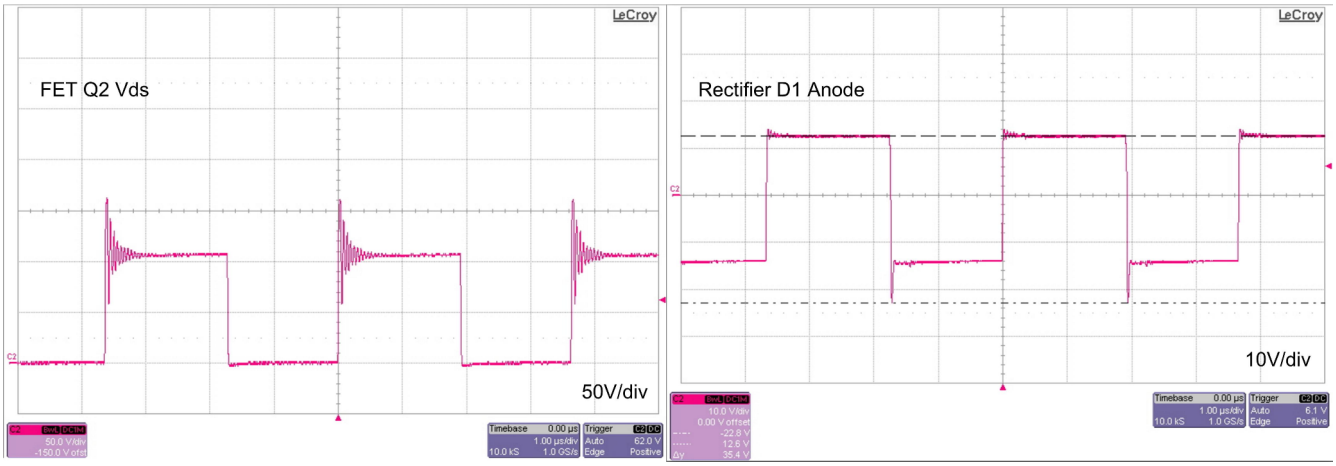

Figure 3. FET and rectifier ringing are limited with a clamp and snubber (57 V_{IN}, 12 V at 5 A).

Flybacks are considered the standard in applications requiring a low-cost, isolated converter. This design example covers basic design considerations for a CCM flyback design.

Check out TI's Power Tips blog series on Power House.

Also see :

- Power Tips #75: USB Power Delivery for automotive systems
- How to design a flyback converter as a front-end for a two-stage LED driver
- LTC Design Note: 560V Input, no-opto isolated flyback converter
- Quasiresonant flyback converter easily charges energy-storage capacitors
- Why use a BJT in a flyback converter?

Technical Article

LLC design considerations for audio amplifiers

Benjamin Genereaux

Special considerations must be taken when designing power supplies for audio amplifiers. The nonlinear nature of audio signals poses a different design challenge compared to standard isolated power supplies. This Power Tip covers the must-knows of designing a half-bridge inductor-inductor-converter (LLC) series resonant converter (HB LLC-SRC) for audio applications.

Audio power

One thing you find in the broad field of electrical engineering is that different industries, or even companies, may use different language to describe the same subject. For a successful design, it is essential for power and audio engineers to understand each other.

Two terms that need be defined first are peak power and continuous power. Peak power is the maximum instantaneous audio power. It will determine how much power to design for the supply to physically output. Continuous power is the audio power averaged over a period of time. In the context of power supply design, continuous power is the specified output power the system can supply without exceeding component temperature or average current ratings. Figure 1 provides an example of the peak and continuous audio levels. They are related by the crest factor, a measure of the ratio of peak to root-mean-square (RMS) value of a waveform.

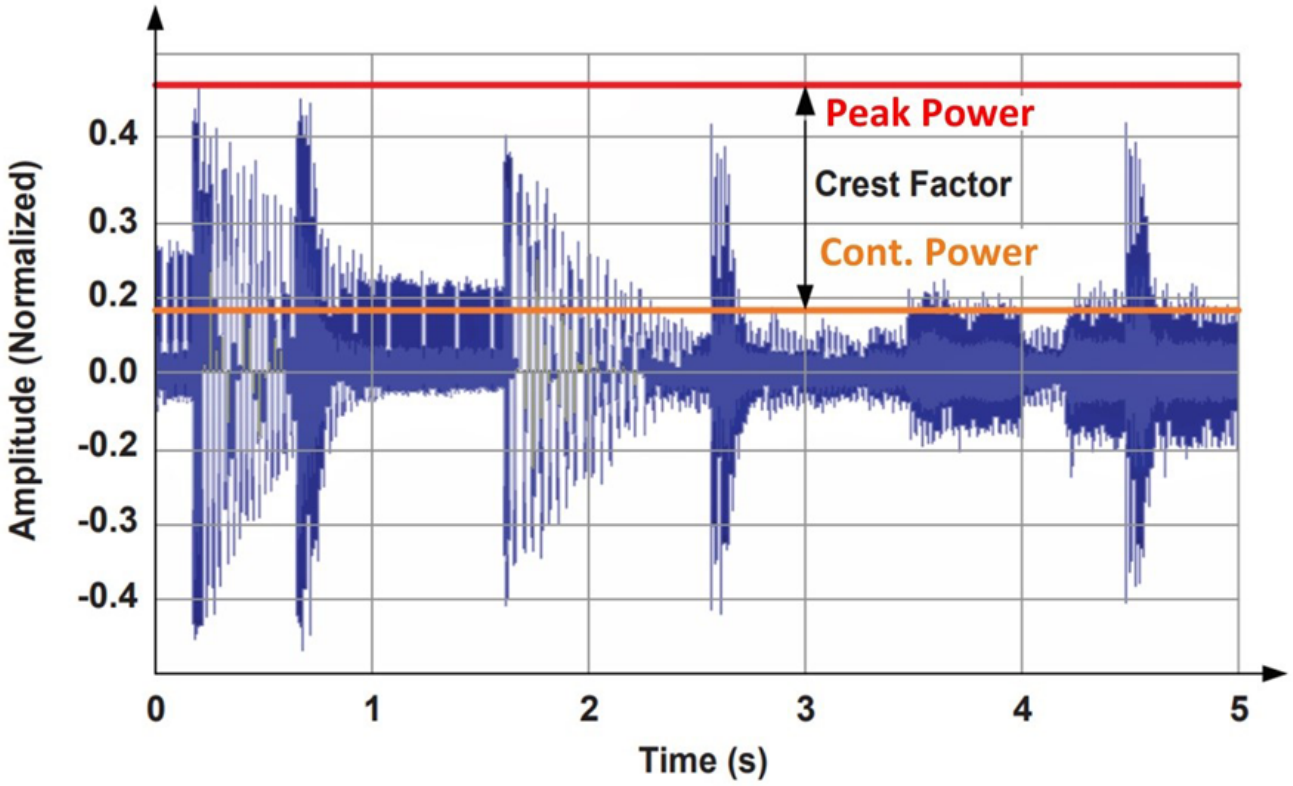

Figure 1. This graph shows continuous and peak power audio levels.

It can also be represented in decibels by Equation 1:

$$C_{db} = 20 \log_{10}\left(\frac{|P_{peak}|}{P_{rms}}\right) \quad (1)$$

RMS is a misnomer in audio power, as the value is not technically the calculated RMS value of the power waveform. Another article could be written on the complexities of how audio amplifiers are specified. Understand that industry standards for rating amplifier power level do not necessarily make clear what the power supply requirements are in terms of peak and continuous power.

As an example, consider an LLC series resonant converter (LLC-SRC) design for a 400-W audio amplifier. Without prior knowledge of audio systems, you may design an excellent 400-W power supply. But when it is time to power up the amp, the supply fails, or audio quality is poor. The LLC converter gain curve will typically be designed based on the maximum load and operate near the series resonant frequency at the minimum line condition. This approach will normally yield a perfectly good 400-W LLC-SRC, but inside an actual audio system peak powers will actually be greater than the 400-W rating of the amp. At a minimum, the continuous and peak power should be specified before starting your power supply design.

For the 400-W amp example, appropriate power levels for a consumer product playing compressed music could be a continuous power of 200 W and a peak power of 800 W for 15 ms. This represents a crest factor of 12 dB, which is typical for processed music. Unprocessed audio will be around 18-20 dB and movie audio can be >20 dB. Ultimately, the ratio of peak to continuous power depends on the specific application, so it is important to clearly define these early in the design process. Time duration requirements for the different load levels are also useful for optimizing the design. Remember that efficiency of the audio amp will need to be considered, as there will be losses in the amp resulting in a higher load on the power supply.

LLC-SRC design

Once the specifications are finalized, you can proceed with the power supply design. Depending on power quality standards of the region and application, you will likely need a power factor correction (PFC) supply for designs of this power level. The PFC front-end will provide a regulated 400VDC bus that serves as the input to the LLC-SRC.

Like most resonant converters, the first step in designing the LLC-SRC is to select the resonant tank components. This will set the resonant frequency and shape the gain curve. At this step, ensure that the output voltage can be reached at the peak power level. If the resonant tank cannot achieve the required gain, then the output voltage will drop at peak audio, reducing audio quality or shutting down the amp. The peak power duration requirement will typically be too long for the output capacitors to hold up the output voltage, so the power supply needs to be capable of actually providing the entire peak load.

Build in some extra headroom on the peak gain. Physical limitations of transformer construction do not always hit the exact number of turns or inductance. For an audio design where it is necessary to reach high peak powers, it is advantageous to use a discrete resonant inductor to ensure a more precise resonant and magnetizing inductance.

At the peak power, it is important to select components rated to handle the peak currents. When designing the magnetics, make sure that they will not saturate. At the continuous power, it is important to select components and packages based on continuous thermal performance. Designers can undersize some of the packages and use the PCB for thermal management rather than a heatsink.

Like any LLC-SRC, shaping the gain curve is an iterative process. Trying to hit certain operating frequencies, resonant currents and voltages and balancing the design between a peak and continuous power level is a challenge. As you go through the calculations, you will need to adjust the magnetizing inductance, resonant inductance, turns ratio and resonant capacitance. 100 kHz is a common resonant frequency target for silicon-based designs. For audio applications it makes sense to target 100 kHz for the continuous power operating point. Figure 2 shows a gain curve shaped for the above example. The operating frequency range is 83–139 kHz.

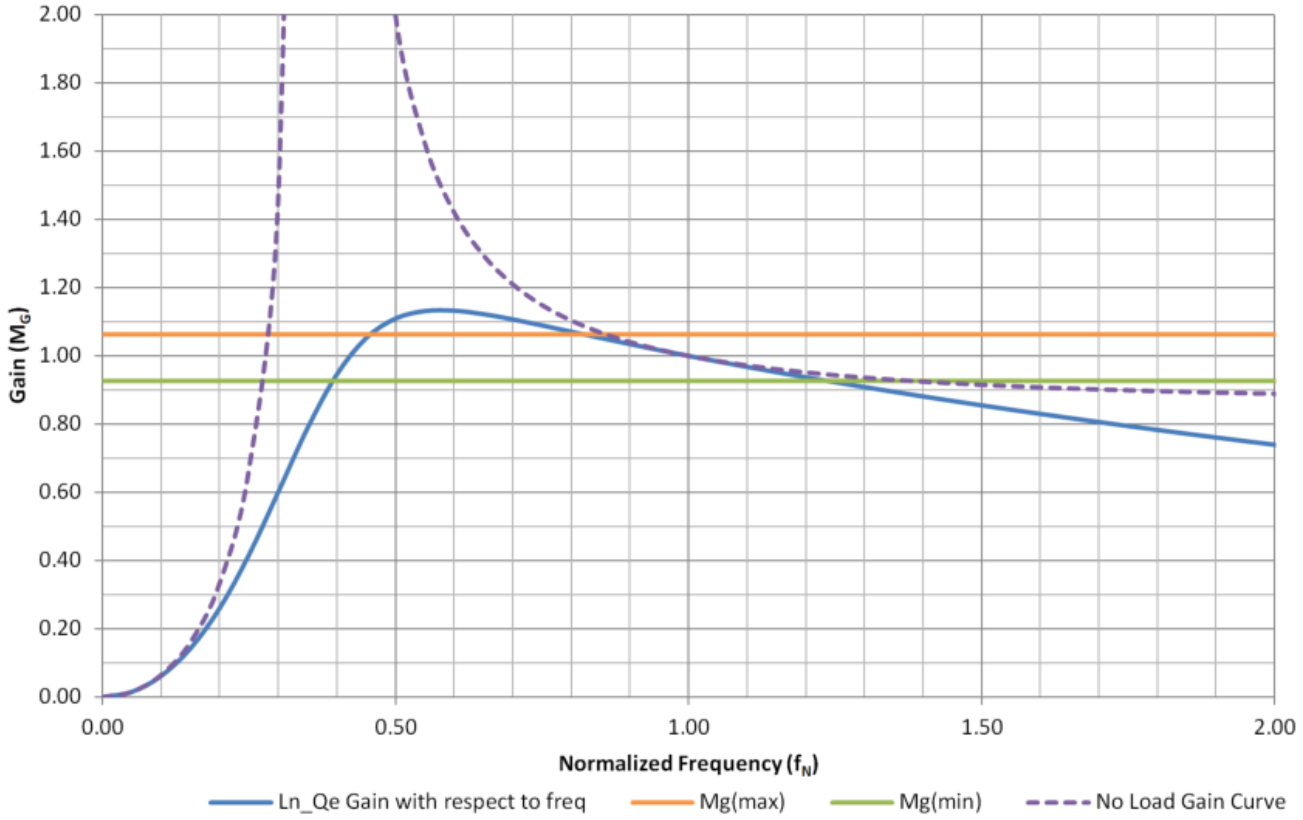

Figure 2. This gain curve is shaped for the LLC-SRC design.

Burst mode

An important aspect of modern LLC-SRC design is burst mode operation for light load efficiency. Burst mode is also used to meet industry standby power regulations. Audible noise is a concern when the burst packet frequency is in the audible noise range, but some LLC resonant controllers like the UCC256404 use a burst mode control law that prevents audible noise generated by the burst frequency. These are three approaches, and possible reasons for choosing them:

1. Enable burst mode: Use burst mode to lower standby power consumption without shutting down the main output. Power will be provided to the amp instantaneously, resulting in no delay due to supply startup.
2. Disable burst mode: In standby, the converter will need to regulate the output with standard switching operation. This decreases light load efficiency, but can reduce complexity and further eliminates any audible noise concerns, such as the effect of the secondary side rectifier parasitics on the gain curve. Figure 2 shows how the gain curve will actually start to rise at higher frequencies. The supply will lose regulation if the minimum gain cannot be reached.
3. External controller disable: Use an external disable circuit to turn off the controller when the audio amp is not running. This lowers standby power further than burst mode but adds cost, as the system now requires an auxiliary power supply. There will also be a startup delay when the amp is ready to output audio.

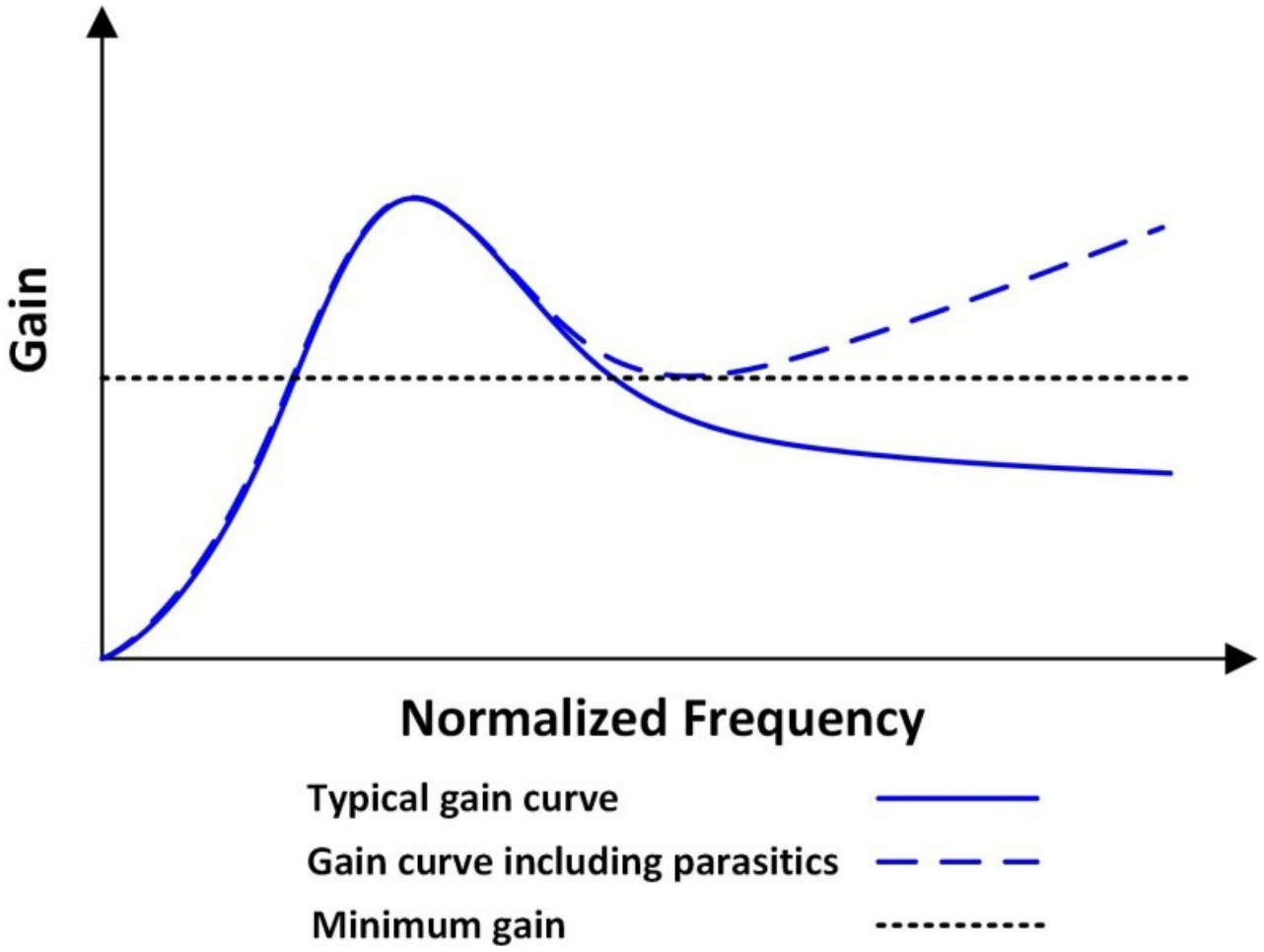

Figure 3. The gain curve will start to rise at higher frequencies with burst mode disabled.

The LLC-SRC is a high-performance topology for continuous power ranges between 100 and 500 W. It is an excellent topology for AC-DC systems that require high efficiency and minimum electromagnetic interference (EMI). Resonant converter design is challenging enough, even before being applied to the intricacies of audio systems. The first step is a mutual understanding between the power and audio engineer on the required peak and continuous power levels of the amplifier. Consider the strategies presented above as a starting point of a successful LLC-SRC design for audio applications.

Sources:

1. Power Solutions for Class-D Audio Amplifiers, Texas Instruments
2. How to Choose a Class-D Audio Amplifier, Texas Instruments
3. Pro Audio Reference, Audio Engineering Society

Related articles

- Power Tips #84: Think outside the LLC series resonant converter box
- Power Tips #97: Shape an LLC-SRC gain curve to meet battery charger needs
- Decibels: Use with caution
- Audio levels, dBu, dBV, and the gang: What you need to know

Technical Article

CLLLC vs. DAB for EV onboard chargers

Brent McDonald

In order to optimize power in electric vehicles (EVs), the onboard charger (OBC) must be highly efficient, light in weight, and small in size. A lighter EV also requires less power to move the vehicle, which increases overall efficiency.

The OBC needs to support an appropriate grid-to-vehicle (G2V) voltage and current battery-charging algorithm; as such, it functions as the power-conditioning interface between the power grid and the EV (Figure 1). In addition, it must be able to provide power from the vehicle-to-grid (V2G) so that the EV can supplement renewable energy sources that might have a fluctuating peak capacity.

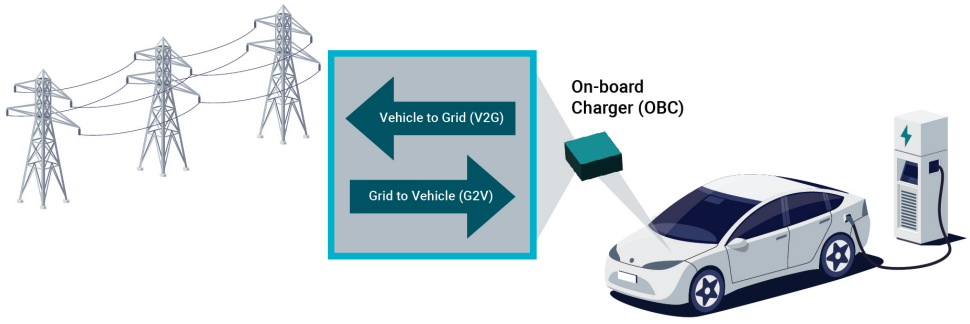

Figure 1. The OBC needs to support an appropriate G2V voltage and provide power from the V2G.

Facilitating the interface between the power grid and the high-voltage battery inside the EV requires an electromagnetic interference (EMI) filter, power factor correction (PFC) and an isolated DC/DC power stage. Figure 2 illustrates this architecture.

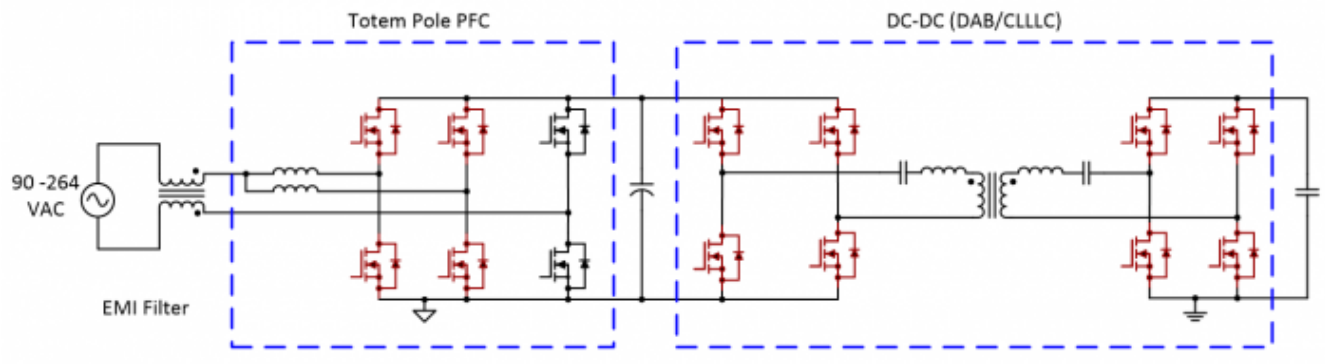

Figure 2. This simplified schematic shows how the OBC serves as the interface between the power grid and the battery.

The scope of this discussion is limited to the DC/DC stage. As of this writing, two popular choices for the DC/DC stage are the capacitor-inductor-inductor-inductor-capacitor (CLLLC) and the dual-active-bridge (DAB) topologies (figures 3 and 4). Both options can achieve a small solution size and provide the necessary G2V and V2G power demands.

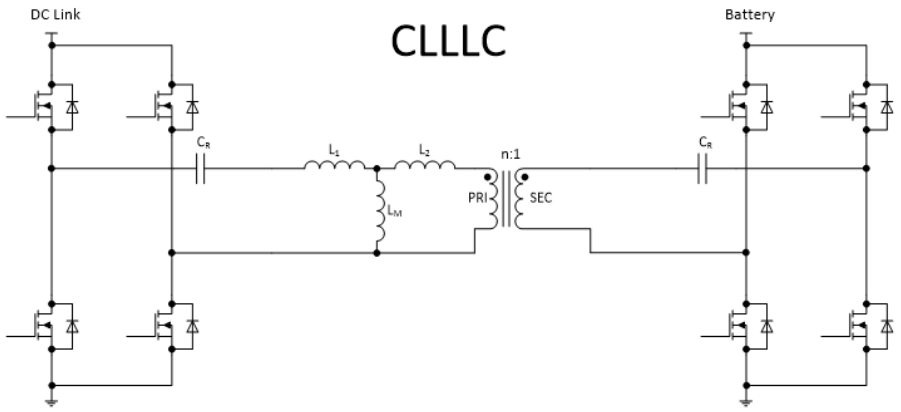

Figure 3. This schematic shows the basic topology of the CLLLC.

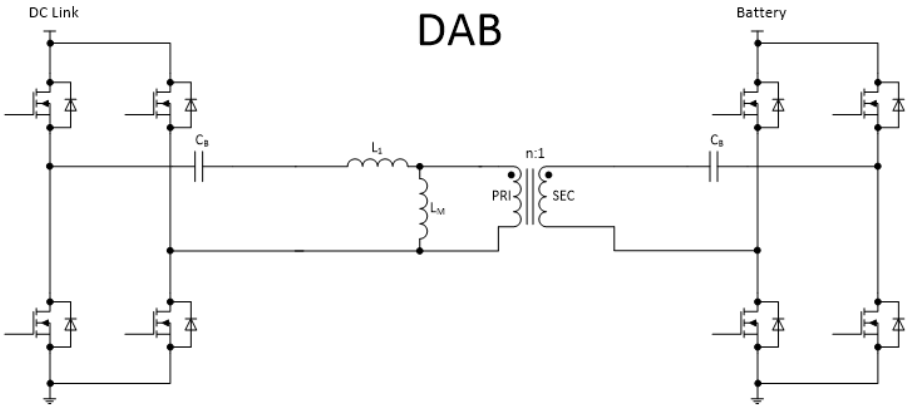

Figure 4. The DAB topology is shown in this schematic.

Maximize OBC performance and minimize its size

To understand how these two topology options can affect the size and performance of the OBC, let's further limit the scope to the battery-charging phase of operation, or G2V, considering how to minimize the charging time by providing the maximum battery power that the switches can tolerate. For example, consider a switch under the following operating conditions:

- P_{DISS} = 20 W
- ϑ_{JA} = 3°C/W
- T_A = 65°C

The switch will have a T_J = 125°C, according to Equation 1:

$$T_J = P_{DISS} \cdot \vartheta_{JA} + T_A \quad (1)$$

The switches in this design cannot tolerate a temperature above 125°C; therefore, this condition represents the highest power level that the OBC can provide to the battery without compromising the switch. The goal is to minimize the power dissipation in the switch and charge the battery as quickly as possible.

Two main factors drive the majority of power losses in the switches: root-mean-square (RMS) current and the switch's ability to maintain zero-voltage-switching (ZVS).

Given their low capacitance and fast turn on and turn off characteristics, Texas Instruments' GaN switches enable the converter to operate at a higher switching frequency than what would be possible with silicon. Higher-frequency operation directly affects the size of the reactive components and results in a smaller transformer, inductors, and capacitors. Let's start by establishing a baseline design for both the DAB and CLLLC, and then explore a circuit enhancement to extend the ZVS range of the converters.

Baseline DAB and CLLLC performance comparisons

Table 1 outlines the basic requirements for the OBC.

Table 1. OBC power requirements.

Description	Min	Typ	Max	Units
AC input voltage	90	220	264	V_{RMS}
AC input current			32	A_{RMS}
DC output voltage	250	400	450	V
DC output current (constant current mode)			20	A
DC output power (constant power mode): >210-V RMS input			6.6	kW

Creating a detailed design for both the DAB and CLLLC helps determine the most viable tank designs. The procedures for doing this are beyond the scope of this discussion; however, circuit simulation is best for adequately approximating the losses in the switches and verifying compliance with the overall functionality. I configured the simulator to run in batch mode over different power levels and input and output voltages and tested different DAB and CLLLC inductor, capacitor, and turns-ratio values. In each simulation run, I collected data on parameters such as VIN, VOUT, switch power, RMS current and switch ZVS conditions. Table 2 summarizes the two optimized topology designs.

Table 2. DAB and CLLLC optimized designs.

Topology	DAB	CLLLC
Tank	$N_P/N_S = 1.1$ $L = 3.3\ \mu H$ $L_M = 20\ \mu H$	$N_P/N_S = 1.1$ $L_{R,1} = 2\ \mu H$ $L_{R,2} = 2\ \mu H$ $L_M = 14\ \mu H$ $C_{R,1} = 50$ nF $C_{R,2} = 50$ nF
Control	Triple phase-shift modulation	Frequency and phase-shift modulation
Variable DC link	400 V to 450 V	400 V to 450 V
f_s	500 kHz	300 kHz-800 kHz

Figure 5 illustrates the salient simulation results. While there are eight switches in each topology, the graphs plot only the switch with the highest power loss. For each switch, there are three plots. The first is the total losses in the switch. The second is the RMS current through that switch. The third plot, on the far right, shows the worst-case drain-to-source voltage that a given GaN switch experiences at turn on. This is a figure of merit of how much ZVS has been lost; the higher this voltage, the larger the losses will be in that switch. Thus, the switch's RMS current coupled with its ability to maintain ZVS represents the greatest portion of power losses in the device.

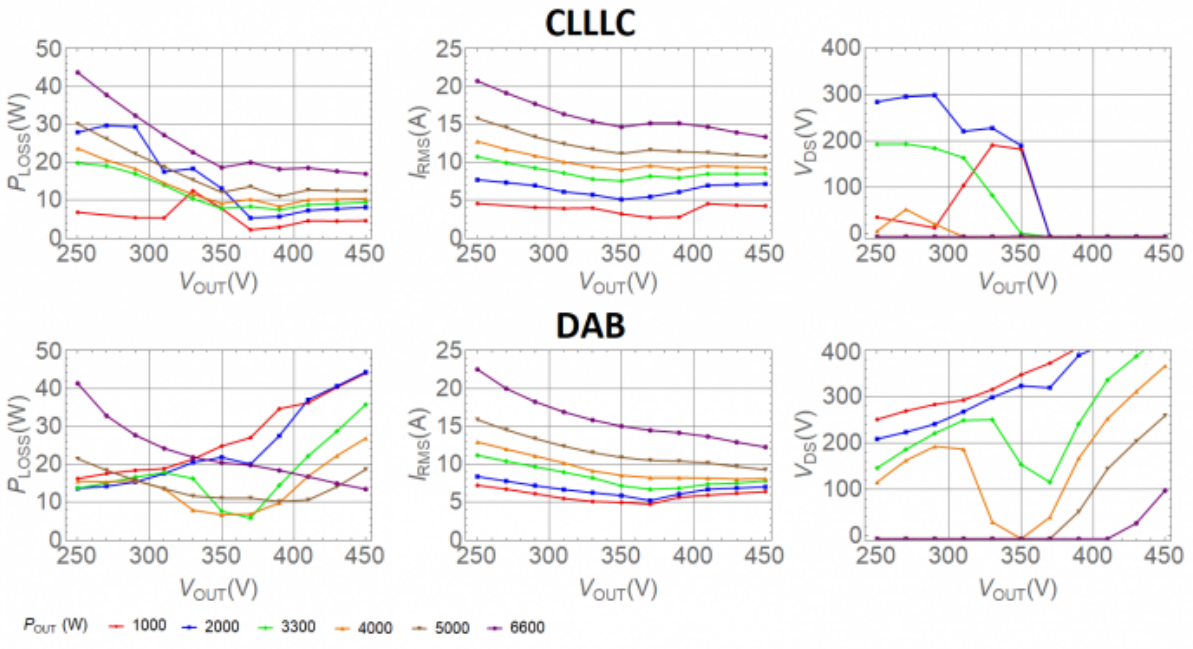

Figure 5. The simulation results show RMS and ZVS baseline conditions for both CLLLC and DAB.

Equipped with these facts and a careful examination of the data, it's clear that the CLLLC is able to maintain ZVS over a wider range of operation. Enhanced ZVS is therefore responsible for the lower power losses seen in the CLLLC switches. Having said that, at 6.6 kW of operation, the DAB has superior performance, which comes from good ZVS and reduced RMS current over most of the range. These observations suggest looking for a way to improve ZVS without adversely impacting the RMS current.

Improving ZVS with commutation inductors

Figure 6 and Figure 7 show the same CLLLC and DAB circuits as figures 3 and 4 with extra inductors (highlighted in yellow) added to the topologies to provide the additional current required to maintain ZVS over a wider range of operation. For now, consider a case when these extra inductors are operational all the time.

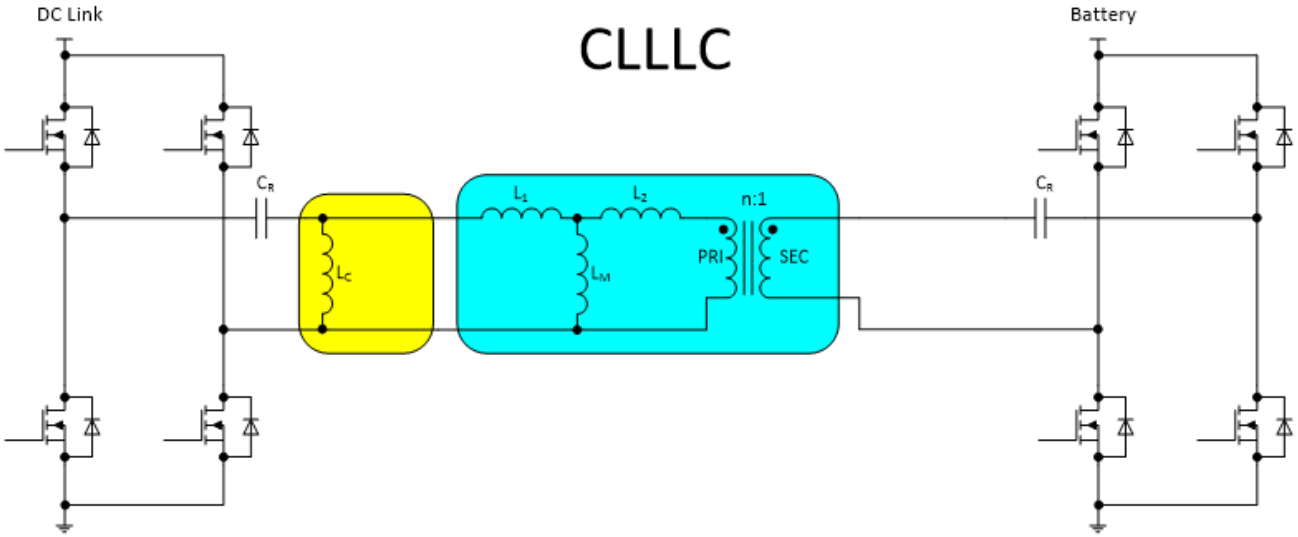

Figure 6. This schematic shows the CLLLC with a commutation inductor.

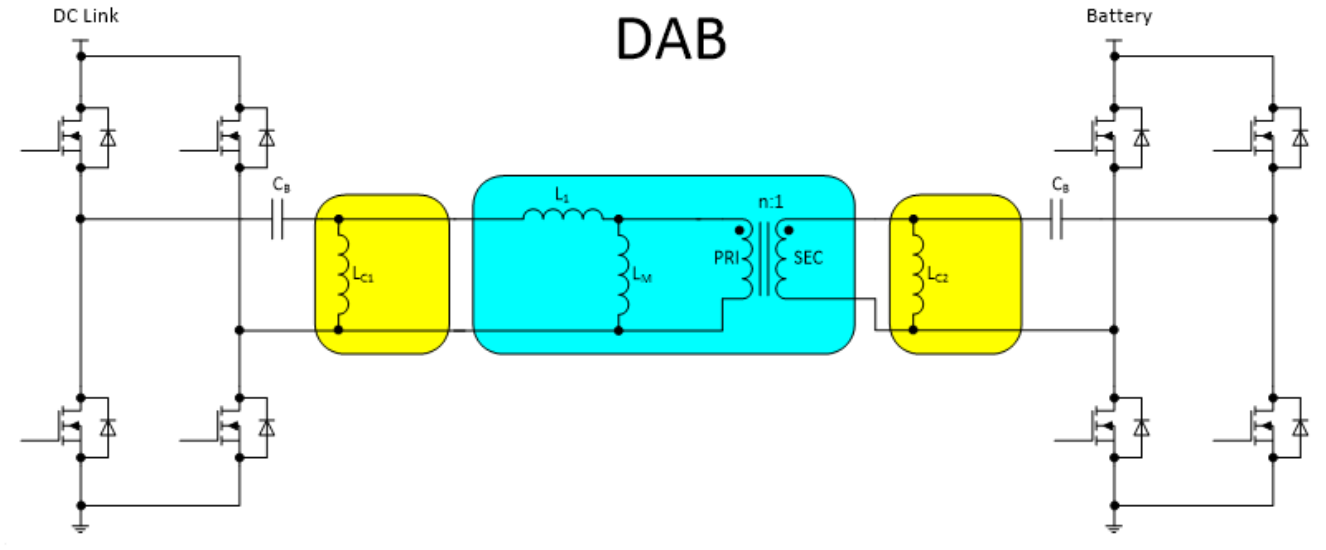

Figure 7. This schematic shows the DAB with commutation inductors.

Table 3 lists the values for the new inductors, and repeats the other tank parameters for convenience.

Table 3. DAB and CLLLC designs with commutation inductor (L_C) values

Topology	DAB	CLLLC
Tank	N_P/N_S = 1.1 L = 3.3 µH L_M = 20 µH **L_C = 20 µH**	N_P/N_S = 1.1 $L_{R,1}$ = 2 µH $L_{R,2}$ = 2 µH L_M = 14 µH $C_{R,1}$ = 50 nF $C_{R,2}$ = 50 nF **L_C = 50 µH**

Figure 8 shows the results after repeating the simulations in Figure 5.

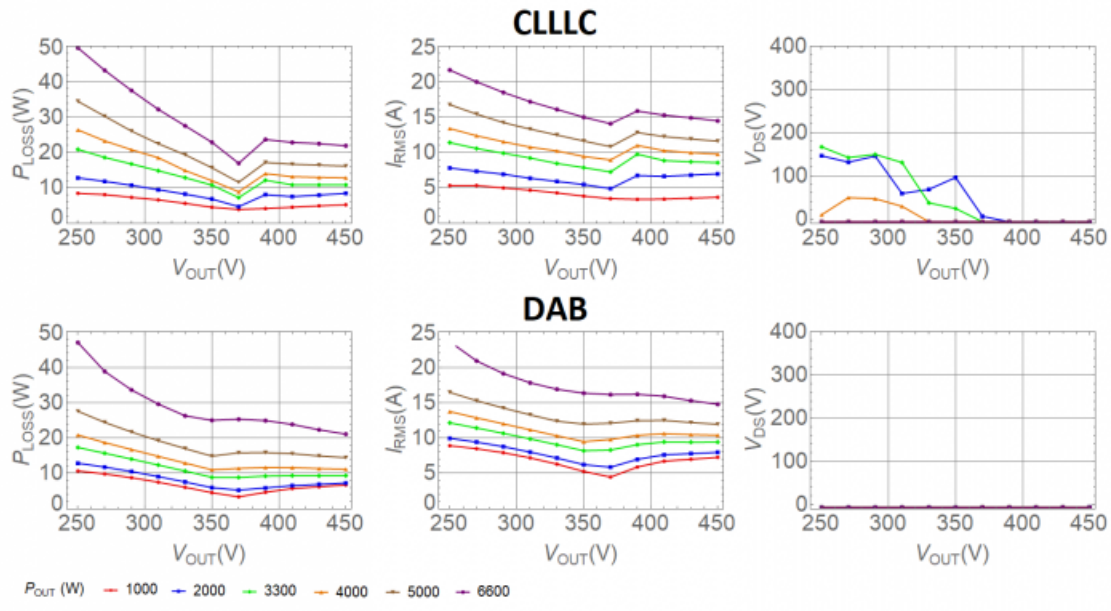

Figure 8. The RMS and ZVS results for each circuit show the impact of L_C.

In this case, notice that the DAB is able to achieve full ZVS over the entire range of operating conditions. This is clearly illustrated by the fact that the V_{DS} of the GaN switch is always at 0V at turn on. The CLLLC, while not achieving full ZVS, is able to achieve significantly improved ZVS. Also notice, however, that the ZVS improvement comes at a significant expense to the RMS currents in both topologies. Looking at the power losses alone, it appears that the DAB converter has the advantage over most of the range.

Before going too far, go back and compare Figure 8 to Figure 5, and you'll notice that under some conditions the commutation inductor actually makes the losses worse. This begs the question – is it possible to create a hybrid approach where you can achieve the lowest of the losses shown in Figure 5 and Figure 8?

Minimizing total losses: have your cake and eat it too

The addition of a commutation inductor creates a broader range of operating conditions where the converter maintains ZVS. This is of tremendous benefit when the converter can't maintain ZVS. The problem with a commutation inductor is that it only improves the losses when ZVS would otherwise be lost. If the converter is already in ZVS, the commutation inductor hurts operation by increasing the current, which results in more ohmic loss in the switches.

This thought process leads to the testing of a hybrid approach where the commutation inductors are left off at the heavier loads and turned on at lighter loads. Figure 9 shows the results after repeating the simulations with this approach, which enables the design to harness each topology's lower RMS currents and natural ZVS ability at heavy loads.

I was careful to add only enough commutation inductance and operation time to fit within the thermal envelope of the switches, in order to prevent unneeded RMS current to the switches or an unnecessary solution size. Note that the DAB converter does not achieve full ZVS over the operating range. The ZVS conditions are much improved, but only as much as they are needed to stay within in the 20-W switch target previously discussed.

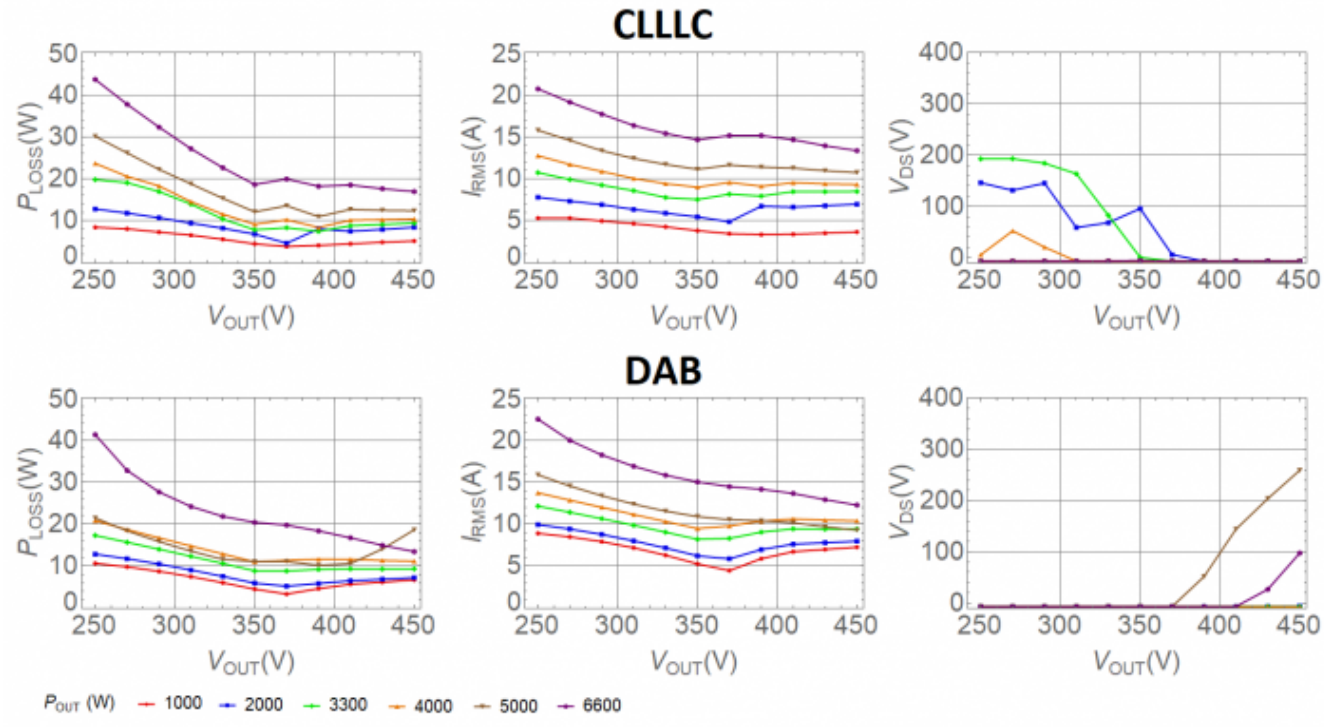

Figure 9. These are RMS and ZVS results using a hybrid approach.

In order to better visualize the trade-offs, Figure 10 summarizes the power losses for each case. You can see that the DAB converter has a clear advantage in terms of power losses in the switch.

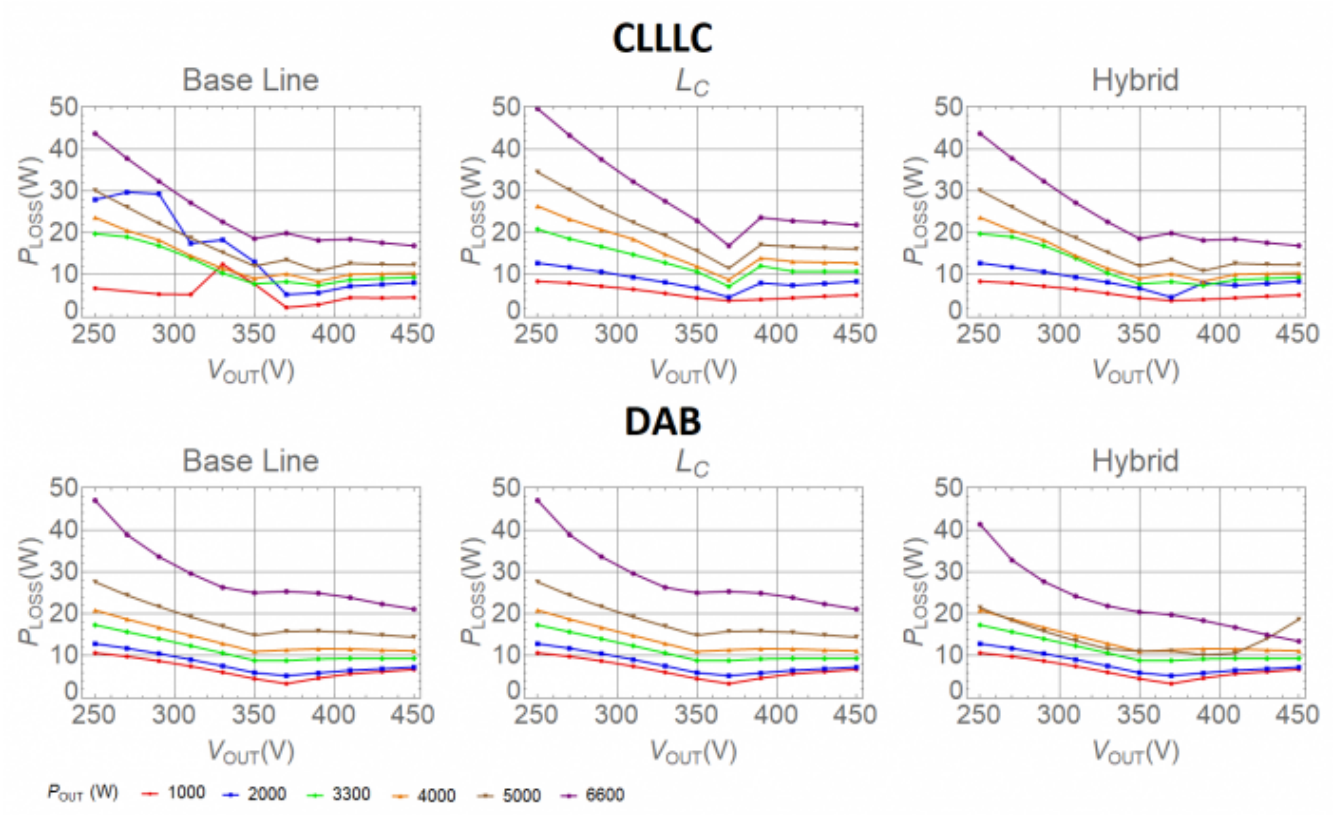

Figure 10. This summary of the power losses for each case helps visualize the trade-offs.

To better illustrate the performance capabilities between these two converters, Figure 11 reformats and plots the data shown in Figure 10. The graph shows the maximum power that each converter can supply, assuming that the switch cannot safely dissipate more than 20 W of power. Remember, 20 W represents the largest loss the switch can tolerate and still keep the junction temperature below 125°C.

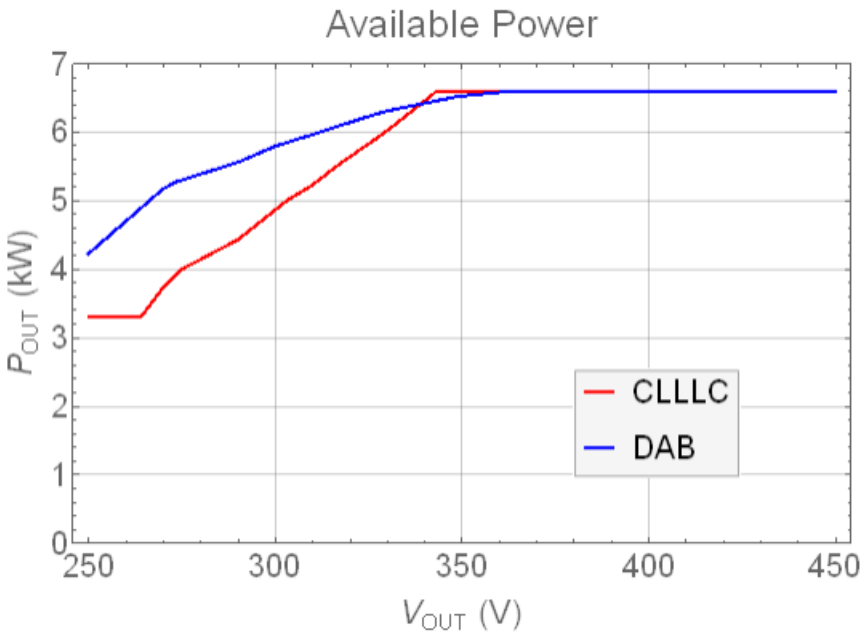

Figure 11. This plot shows the maximum power that each converter can supply.

Is CLLLC or DAB better?

As evidenced by the fact that the blue line is above the red in Figure 11, the DAB converter can provide more power over the entire range than the CLLLC. This makes it tempting to assume that the DAB is the clear winner. However, remember that minimal size and weight are central requirements of an OBC. The DAB converter needs two extra inductors, but the CLLLC only needs one. In my opinion, that gives the win to the CLLLC.

Like most things in engineering, what's best is almost always a matter of trade-offs against the requirements. It's pretty rare that big advantages come for free, and in this case it's no different. To me, the CLLLC edges out the DAB because it appears to have a clear size advantage.

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Technical Article

Get more boost from your boost converter

John Betten

Boost converters provide a higher output voltage from a lower input voltage. Getting the most “boost” possible requires maximizing the operational duty cycle.

Boost controllers have a limit on their maximum continuous duty cycle, which is typically highest at lower switching frequencies. If you exceed this maximum duty cycle, pulse skipping occurs, which is generally detrimental and should be avoided. Many controllers have maximum duty cycles in the 80% to 90% range, which may increase by a few percent if they’re operated at a very low switching frequency. Low switching frequencies require larger components and increased circuit board area. But even when operating at low switching frequencies, you still might not be able to get enough boost. So what can you do?

Figure 1 shows a simplified schematic of a traditional boost converter power stage. Its main benefit is its low component count, standard inductor and ability to implement a simple low-side boost controller. A key limitation of this basic boost, however, is that it can only provide a maximum boost ratio of 10-to-1, assuming a 90% maximum duty cycle. If you need more boost, you could try using a flyback or boost converter with a charge-pump doubler. Charge pumps added to a boost are good for low output currents, but require additional components to implement. Flybacks are a reasonable solution as well. But an even simpler solution exists with fewer transformer pins, lower turns ratios and lower leakage inductance.

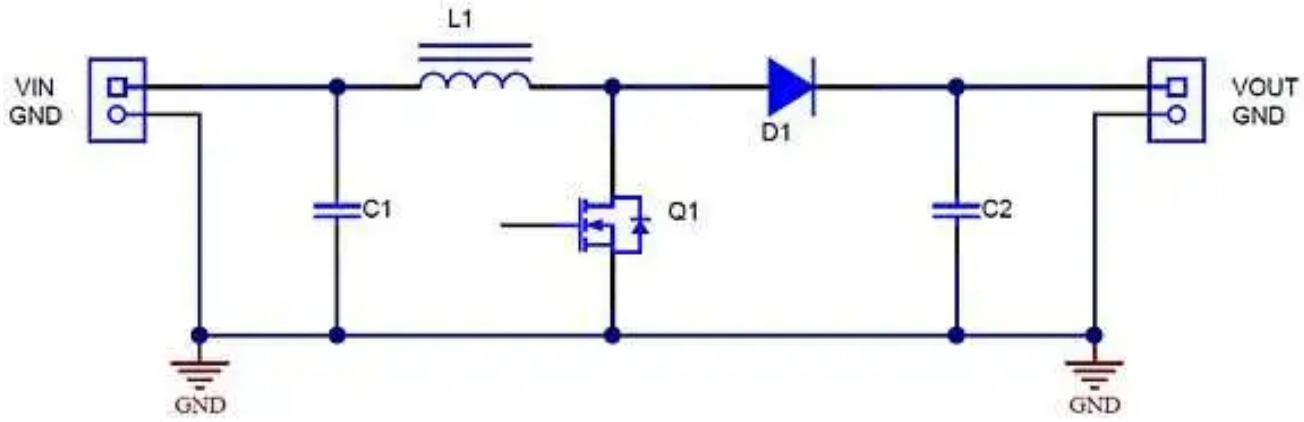

Figure 1. A traditional single inductor boost converter power stage.

Figure 2 shows an autotransformer boost converter. It uses two series-connected windings on the same core, which behaves as a transformer without isolation. Placing the primary in series with the secondary reduces the required turns ratio compared to a flyback, while also requiring fewer pins.

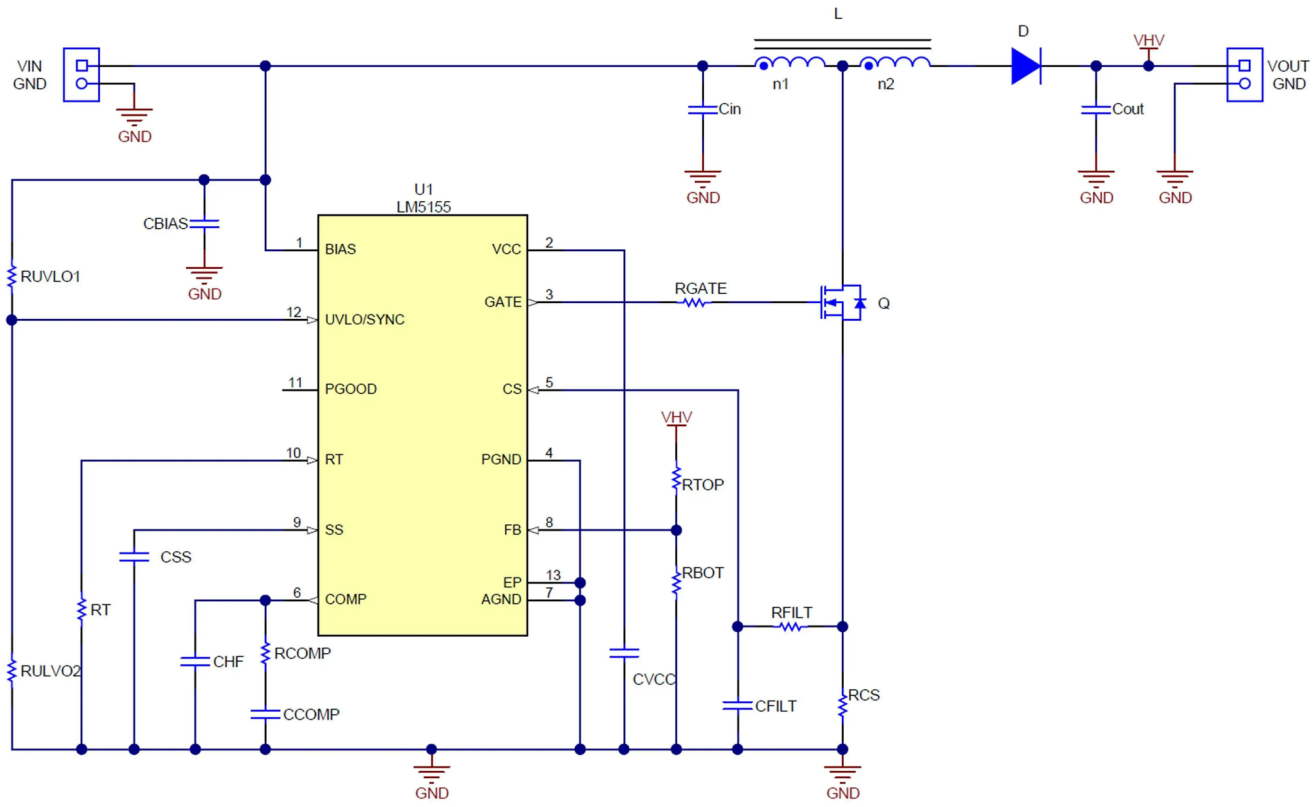

Figure 2. An autotransformer boost converter provides a higher output voltage than a traditional boost.

Equation 1 expresses the duty cycle for operation in continuous conduction mode (CCM) for a given Vin, Vout and n2/n1 turns ratio (ignoring the field-effect transistor [FET] and current-sense resistor drops):

$$d = \frac{Vout - Vin + Vd}{\frac{n2}{n1} \times Vin + Vout + Vd} \quad (1)$$

You can see that for a large n2/n1 turns ratio, the duty cycle decreases. This is beneficial for providing a higher output voltage. Equation 2 solves the expression for Vout:

$$Vout = \frac{Vin \times \left(1 + d \times \frac{n2}{n1}\right) - Vd \times \left(1 - d\right)}{1 - d} \quad (2)$$

You can see that if n2/n1 = 0, the expression is the same as it is for a traditional boost converter. So for a non-zero n2/n1 turns ratio, Vout increases by an additional amount equal to (n2/n1)*Vin*d/(1-d), so much higher output voltages are possible.

Figure 3 plots the boost ratio, Vout/Vin, versus the duty cycle for several n2/n1 turns ratios, including zero for a traditional boost for comparison. At a 90% duty cycle, the traditional boost has a ratio of 10 compared to 19 for n2/n1 = 1, allowing nearly two times the output voltage. You can easily implement a 1-to-1 n2/n1 ratio with a standard coupled inductor, many of which are readily available. Larger turns ratios can provide a substantially higher output voltage.

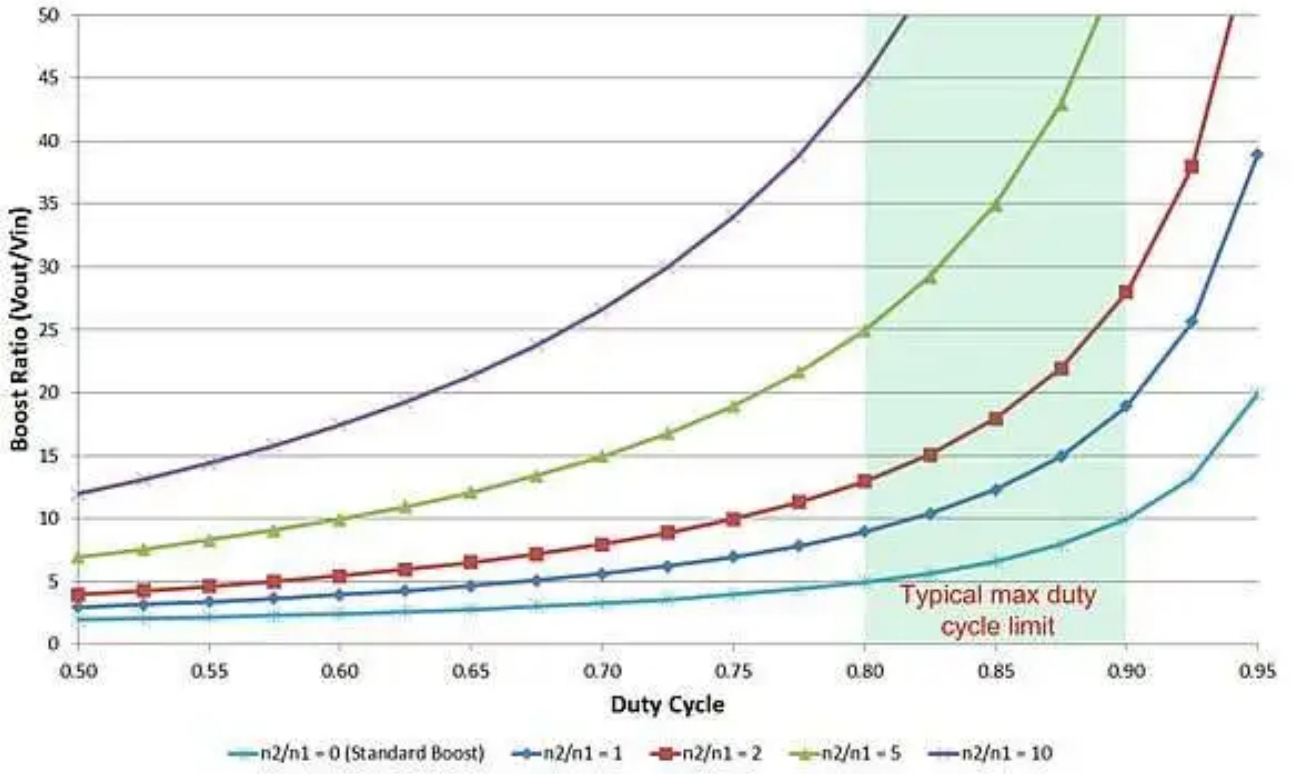

Figure 3. Tapped inductors reduce duty cycles and enable higher output voltages.

You will usually know the boost ratio based on design specifications. The maximum practical duty cycle is determined by the controller chosen and the desired switching frequency. Figure 4 shows you how to easily determine the required turns ratio. For example, suppose you need 250 V out from a 10-V input, and wish to limit the maximum duty cycle to 80%. Select the boost ratio of 250 V/10 V = 25 and follow it to the blue curve (d = 0.8); the required n2/n1 is 5.

Equation 3 shows voltage stress for the FET when off, while Equation 4 shows the rectifier reverse voltage stress:

$$Vfet = Vin \times \left(1 - \frac{n1}{n1 + n2}\right) + \left(Vout + Vd\right) \times \frac{n1}{n1 + n2} \quad (3)$$

$$Vdiode = Vout + Vin \times \frac{n2}{n1} \quad (4)$$

For the design example above, the FET and rectifier voltage stresses are 50 V and 300 V, respectively. The FET voltage stress is considerably lower than a traditional boost, which would have about 250 V across it. Since leakage inductance will be present, an resistor-capacitor snubber may be necessary to reduce ringing.

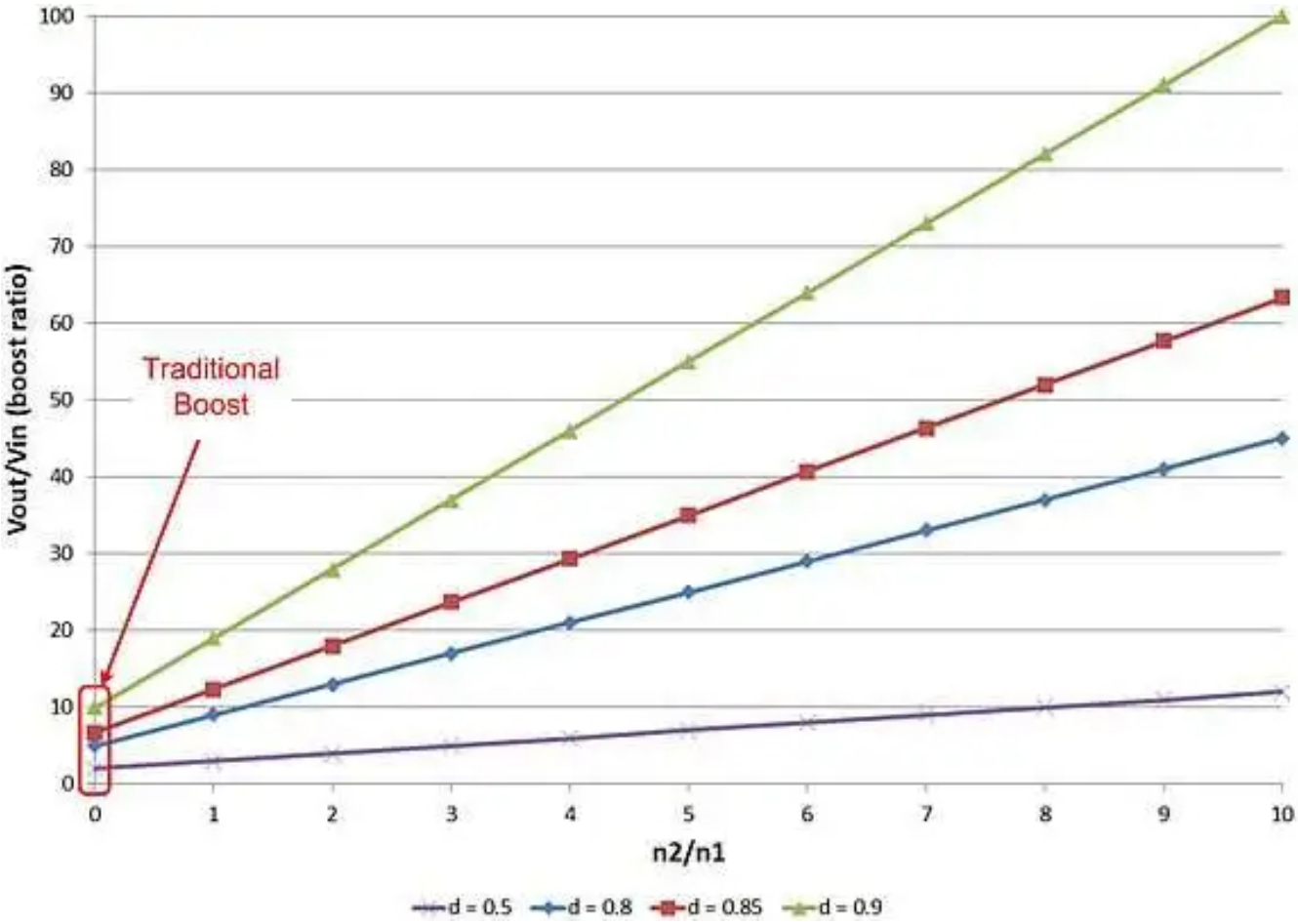

Figure 4. Determine your required turns ratio by selecting your boost ratio and maximum duty cycle.

Implementing an autotransformer in a CCM boost converter provides several advantages. It increases the output voltage possible beyond that of a traditional boost converter with only the addition of a winding. It reduces the operational duty cycle, enabling higher switching frequencies, smaller component sizes and a lower FET voltage. A reduced duty cycle may also offer a broader selection of controllers that previously could not operate at sufficiently high duty cycles when implemented in a traditional boost converter.

For more Power Tips, check out TI's Power Tips blog series on Power House.

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Technical Article

How to improve flyback efficiency with a nondissipative clamp

Brian King

In the standard form of a flyback converter, the leakage inductance of the transformer creates a voltage spike on the drain of the primary field-effect transistor (FET). Preventing this spike from becoming excessive and damaging, the FET requires a clamping network, usually with a dissipative clamp, as shown in Figure 1. But the power lost in dissipative clamps limits flyback converter efficiency. In this Power Tip, I will investigate two different variations of the flyback converter that use nondissipative clamping techniques to recycle leakage energy and improve efficiency.

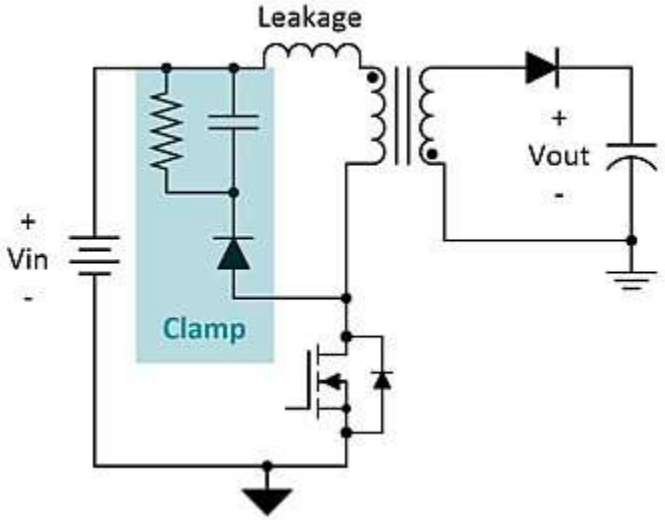

Figure 1. Most flyback converters employ a dissipative clamp.

The power lost in a dissipative clamp is related to energy stored in the leakage inductance of each switching cycle. When the FET is on, the current in the primary winding of the transformer increases to a peak current value determined by the controller. This peak current is flowing in both the primary magnetizing and leakage inductances. When the FET turns off, the magnetizing energy is delivered to the output through the secondary winding of the transformer. The leakage energy is not coupled through the transformer core, so it remains on the primary side and flows into the clamp.

It is important to understand that not only is the leakage energy dissipated in the clamp; so is a portion of the magnetizing energy. As discussed in Power Tip #17, clamping the primary winding voltage much higher than the reflected output voltage minimizes the amount of magnetizing energy burned in the clamp.

The two-switch flyback is a common variation of the flyback converter that reclaims the leakage energy. Figure 2 is a simplified schematic of a two-switch flyback. The two primary FETs are connected in series with the primary winding between them. These two FETs are simultaneously either on or off. When they are on, the primary winding connects to the input and is energized to a peak current. When they turn off, the secondary winding delivers the magnetizing energy to the output, and the leakage energy is recycled back to the input through D1 and D2. By reclaiming the leakage energy, two-switch flybacks boast higher efficiency than their single-switch dissipative clamp counterparts.

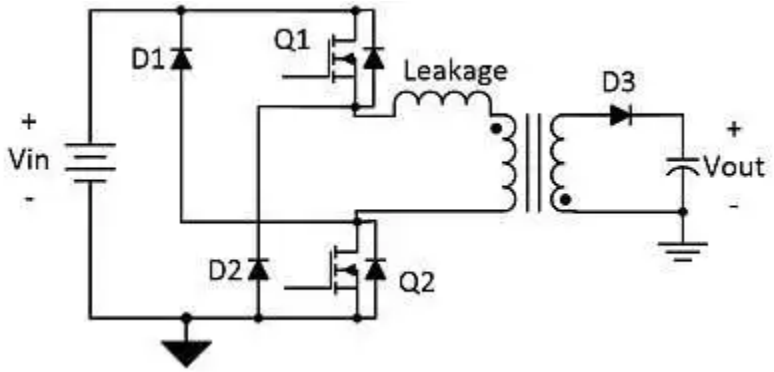

Figure 2. The two-switch flyback recycles leakage energy to the input.

The efficiency gained is somewhat offset by the fact that two switches are conducting simultaneously, so conduction losses tend to increase, especially in low-input-voltage applications. Luckily, the drain-to-source voltage of both FETs clamp to the input voltage, so you can use lower-voltage-rated FETs compared to a single-switch flyback. The clamped voltage stress is also advantageous in high-input-voltage applications.

The efficiency gain is related to the ratio of the leakage inductance to the magnetizing inductance, and is typically around 2%. Reclaiming the leakage energy has benefits other than higher efficiency. In high-power flyback applications (generally greater than 75W), losses in a dissipative clamp can create a thermal management nightmare. The two-switch flyback completely eliminates this heat source.

The trade-off for this higher efficiency and improved thermal performance comes in the form of increased cost and complexity. Not only is an extra FET required, so is an isolated drive for the high-side FET. Additionally, the transformer turns ratio needs to be set such that the reflected output voltage is less than the minimum input voltage. If not, the output voltage will be clamped and the transformer will not properly reset. As a result, the two-switch flyback is inherently limited to a maximum 50% duty cycle. In reality, the reflected output voltage should be sufficiently lower than the minimum input voltage to allow the leakage inductance to reset quickly.

The circuit in Figure 3 shows another way of reclaiming the leakage energy, but using a single-switch flyback. This nondissipative clamp is not new, but it is not well-known either. It provides many of the same benefits as the two-switch flyback.

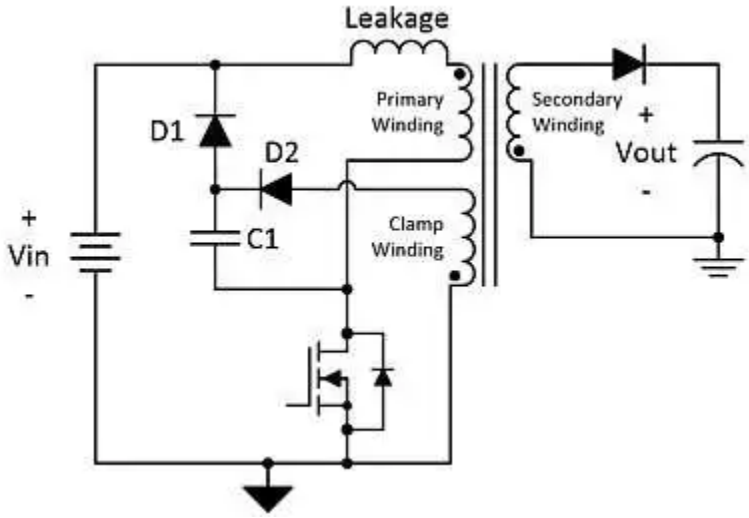

Figure 3. A simple nondissipative clamp added to a single-switch flyback.

Implementing this clamp requires adding a clamp winding on the primary side of the transformer. This winding must have the same number of turns as the primary winding. A clamping capacitor is added, tied to the drain of the FET. The other end of the clamp capacitor is clamped to the input voltage by diode D1 and to the clamp winding by diode D2.

The clamp winding and D2 limit the voltage across the clamp capacitor to a maximum value equal to the input voltage, evident when applying Kirchoff's voltage law around the primary loop, as shown in Figure 4. Notice that the two primary winding voltages cancel each other regardless of the polarity or magnitude. This method only works when using the same number of turns on both windings.

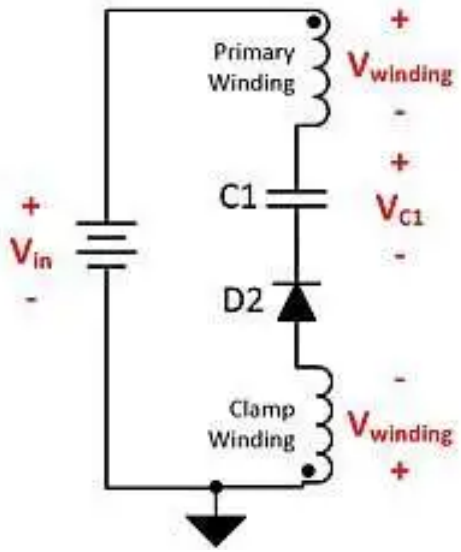

Figure 4. The clamp capacitor voltage is limited by the input voltage.

To understand how this clamp works, consider what happens when the FET turns off. When the primary FET turns off, current in the leakage inductance flows through the clamp capacitor and forward-biases diode D1. While D1 is on, the leakage inductance will have a voltage across it equal to the difference between the input voltage and the reflected output voltage. Once the current in the leakage inductance drops to zero, D1 turns off. The leakage energy delivered into the clamp capacitor temporary increases the voltage on the clamp capacitor slightly above the input voltage. When D1 turns off, the D2 clamp effectively transfers this stored charge to the output through the coupling in the transformer windings.

This clamp circuit requires fewer components and is cheaper than a two-switch flyback. Just like the two-switch flyback, it provides an efficiency improvement of a few percent and eliminates thermal issues related to dissipating the leakage energy. This clamp circuit also limits the duty cycle to a 50% maximum. The trade-off is that the circuit requires a higher-voltage FET, which must be rated for more than twice the input voltage. The higher voltage on the drain of the FET may also present more of a challenge for electromagnetic interference than a two-switch flyback.

The active-clamp flyback is another version of flyback that reclaims the leakage energy and at the same time can provide zero voltage switching. The active clamp flyback is more complicated and requires a specialized controller, such as the UCC28780, making it worthy of its own Power Tip, so I'll save that discussion for later. The next time you are designing a high-power flyback, consider employing a nondissipative clamp to improve your efficiency and keep your power supply cool.

Related articles

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Technical Article

Two simple isolated power options for 8 W or less

Josh Mandelcorn

A variety of industrial and automotive systems use isolated bias supplies. Most existing approaches using flyback or push-pull converters for isolated bias power (see the Texas Instruments [TI] "Isolated Bias Power Supply Architecture and Topology Trade-Offs for HEV/EVs" presentation and "HEV/EV Traction Inverter Power Stage with 3 Types of IGBT/SiC Bias-Supply Solutions Reference Design") require significant design effort and rely on a low leakage inductance isolation transformer.

In this power tip, I'd like to present two approaches that both reduce design complexity and noise coupling in isolated bias supplies. One approach, useful for multiple isolated outputs and overall output power to 8 W, uses the inductor-inductor-capacitor (LLC) topology along with a half-bridge driver such as TI's UCC25800-Q1. The second approach, which integrates the isolation transformer and is useful for up to 1.5 W and one isolated output, uses a single integrated circuit (IC) such as TI's UCC14240-Q1. That device contains both the power and feedback isolation and needs only filter capacitors and resistor-dividers to complete the design.

The complexity of isolated power, especially at low power levels, is a significant cost-, size- and design-resource burden. The most common topology for low power is the flyback converter. Conventional flyback converters use an optocoupler to feed back the output voltage from the secondary side to the controller IC on the primary side. Low-cost optocouplers are not an option in demanding automotive and industrial environments because of long-term reliability concerns. Even with closed-loop regulation, only one of the flyback outputs is really fully regulated. Flyback converters with primary-side regulation that eliminate any optocoupler requirement, such as TI's LM5180-Q1, are available. However, the need for a low-leakage transformer, with its noise and isolation challenges, remain.

With most converter topologies, a low-leakage transformer is key to delivering power across the isolation barrier efficiently. Methods to reduce transformer leakage inductance, such as closely coupled windings and interleaving, generally increase the primary to secondary capacitance. This capacitance spreads noise from both the isolated converter switching itself, and the circuitry to which the isolated output is connected, such as a high-side switch in a traction inverter or an onboard charger. These switches can swing up and down at over 100 V per nanosecond. Also, there is a significant cost and size burden in transformers requiring both high (several kilovolts) reinforced isolation and low leakage inductance.

My focus here will be on the highly isolated power needs of approximately 8 W or less, where the available primary-side power is in the range of 12 V_{DC} to 24 V_{DC}. A high isolation rating (3-kV root mean square [RMS] or greater) is necessary to meet safety isolation where power is needed in circuitry connected to the AC mains or to 400- and 800-V batteries. Application examples include isolated bias power in onboard chargers for electric vehicles and traction inverters, which typically need roughly +15 V for rapid switch turnon and roughly –5 V for rapid switch turnoff, with the return tied to the emitter or source of the high-power switch.

One IC for multiple outputs and up to 8 W: the UCC25800-Q1

The LLC topology (see the application note, "Bias Supply Design for Isolated Gate Driver Using UCC25800-Q1 Open-Loop LLC Transformer Driver") allows good load regulation of the isolated output voltage without feedback. This topology actually uses the leakage inductance of the transformer to provide soft switching and greatly reduce switching losses in the main switches. The fact that the leakage inductance effect on output regulation can be effectively tuned out by the coupling capacitance allows the use of high isolation transformers, on which the primary and secondary are on separate bobbins. This results in very low coupling capacitance for low system noise and high reinforced (several kilovolts) isolation for safety purposes. The soft switching, combined with the tuning out of the leakage inductance by the coupling capacitor, turns leakage inductance from being an enemy to being a friend.

This approach does require a regulated input DC voltage for power to avoid the need for secondary-side regulation. With a two-switch half bridge (for the low power levels needed here), a square wave of one-half the input voltage is applied to the transformer primary. For automotive applications, there is often a regulated DC voltage of 12 V or 24 V for other purposes. If a pre-regulator is necessary, a simple single-ended primary-inductor converter will provide the regulated 15- or 24-V input power. The design burden of this pre-regulator will often be much less than the challenge of taming the system noise caused by the low-leakage flyback transformer.

Published design examples with the UCC25800-Q1 include the "Pre-Regulated Isolated Driver Bias Supply Reference Design for Traction Inverter Applications": four outputs, 6 W total off 30 V (shown in Figure 1 and Figure 2) and the "Isolated IGBT and SiC Driver Bias Supply Reference Design for Traction Inverter Applications," with +16 V/–5V for 6.6-W maximum off of 24 V. The transformer used in the insulated-gate bipolar transistor (IGBT) and silicon carbide (SiC) driver reference design has only 1.3-pF typical of primary to secondary capacitance, versus 20-pF typical for a flyback transformer of similar power. This reduction by more than a factor of 10 in capacitance represents at least a 20-dB reduction of noise spread in the system. The only primary and secondary interfaces are the transformers.

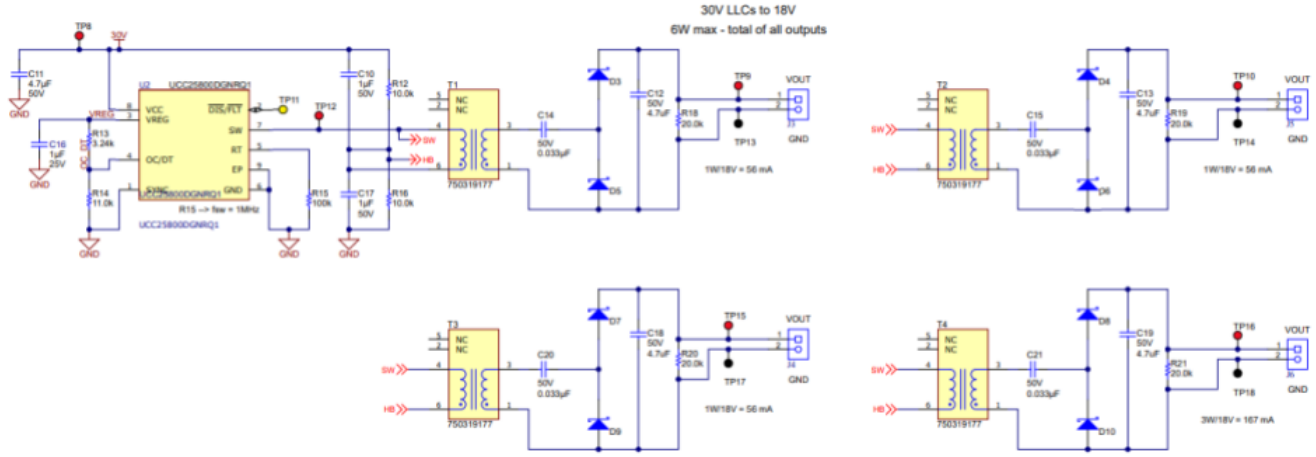

Figure 1. From the pre-regulated reference design schematic—the isolated four-output converter. Source: Texas Instruments

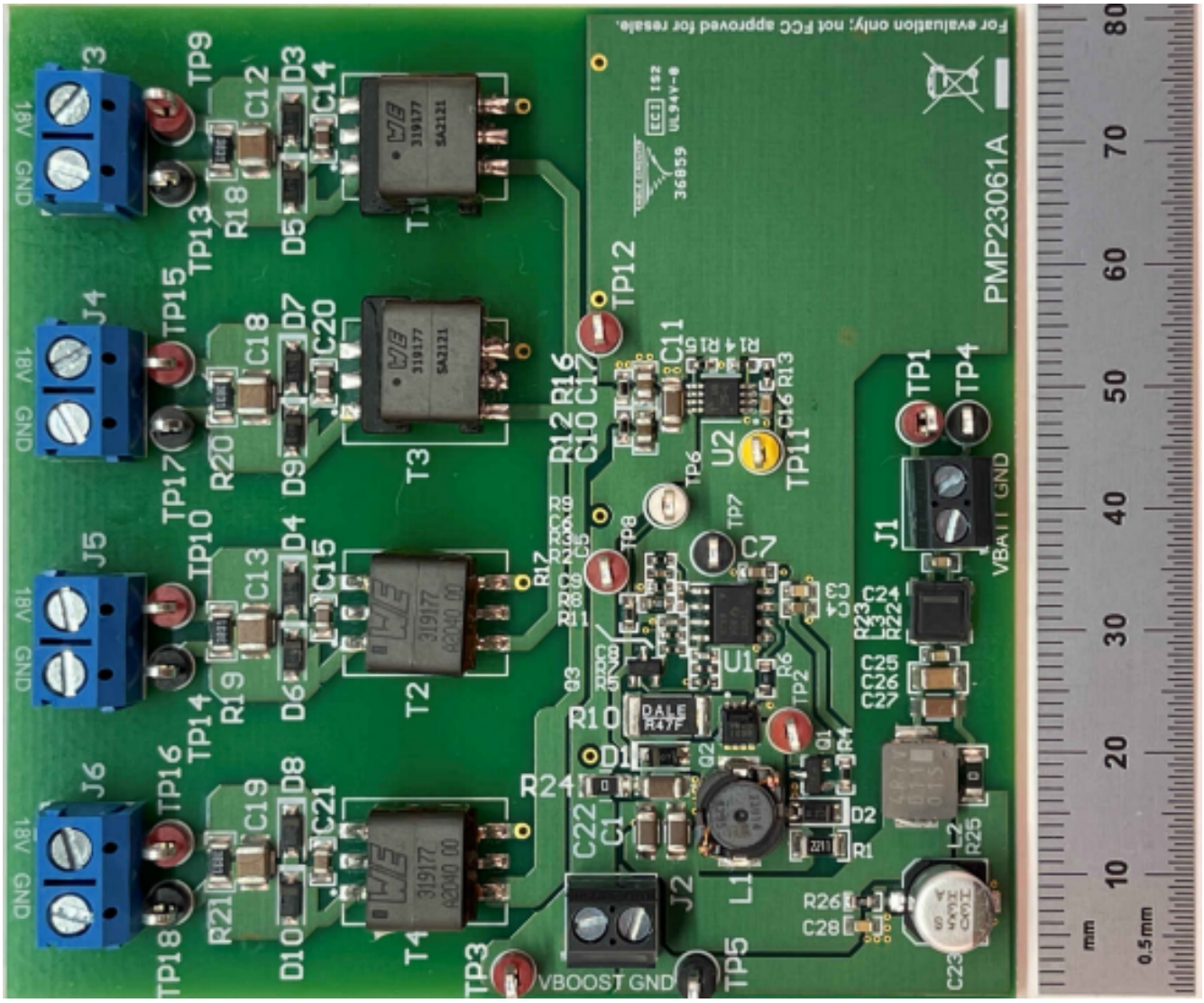

Figure 2. Pre-regulated reference design assembled board, including boost circuit from 6 V_{IN}. Source: Texas Instruments

Output regulation of the four outputs varied in range from 16.25 V to 17.27 V for loads from 10% to 100% of the maximum load.

A simpler approach when you need less than 2 W of isolated power: the UCC14240-Q1

An even simpler approach is a self-contained isolated converter IC that integrates the transformer and secondary to primary feedback, with only the input/output capacitors and voltage dividers needed to set both the positive and negative outputs. The power stage includes a primary-side full bridge, an isolation transformer with very low primary to secondary capacitance of approximately 3.5 pF to minimize system noise coupling, and a full-bridge output rectifier. Choosing a switching frequency of 13 MHz both enables this low primary to secondary capacitance and keeps its own switching noise well removed from any bands of concern in automotive applications. The internal feedback of the IC allows the input voltage to vary more than ±10% from nominal and still give well-regulated positive and negative voltages to within 1.3% of nominal output. This IC shows that topology complexity - which is fully contained inside the IC – is not a design burden.

The UCC14240-Q1 works off 21 V_{IN} to 27 V_{IN} and targets gate-drive applications for IGBTs and SiC metal-oxide semiconductor field-effect transistors in traction inverters, onboard chargers and motor control, with a typical positive voltage of +15 V to turn on the device, and a typical negative voltage of –5V to turn off the device. However, other combinations of positive and negative voltages are allowed within the 18-V to 25-V total.

Figure 3, Figure 4, and Figure 5 illustrate a self-contained high-isolation example with planned 3,000-V_{RMS} isolation as part of an "SPI-Programmable Gate Driver and Bias Supply Reference Design." U1 is the actual DC/DC isolated power supply, U3 is a smart isolated gate driver, and U2 with Q1 and L1 is a car battery to DC converter. Note the 8-mm primary-to-secondary isolation valley.

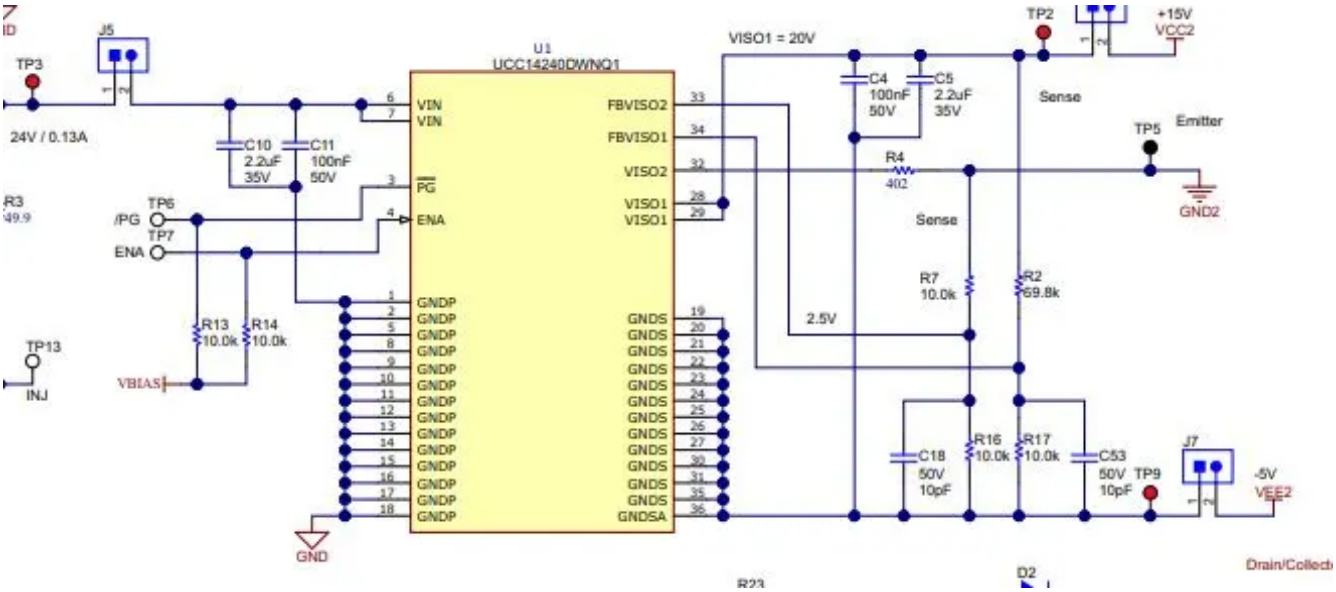

Figure 3. From the automotive "SPI-Programmable Gate Driver and Bias Supply with Integrated Transformer Reference Design" schematic - the isolated +15-V/–5-V converter. Source: Texas Instruments

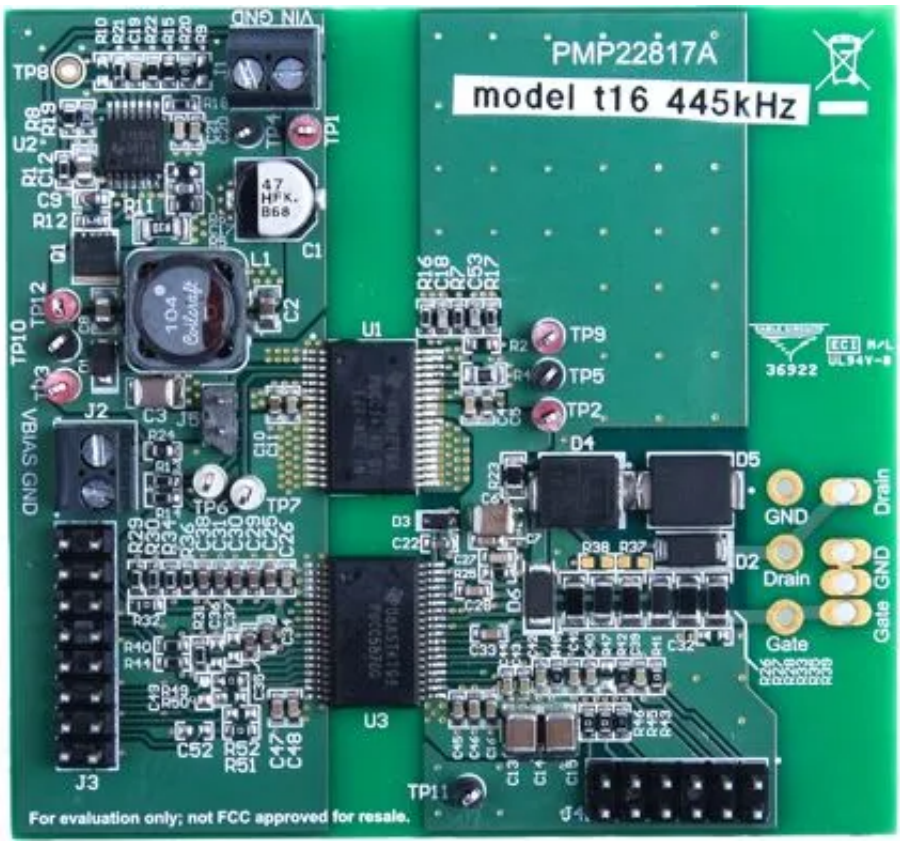

Figure 4. Automotive SPI-programmable reference design assembled board. Source: Texas Instruments

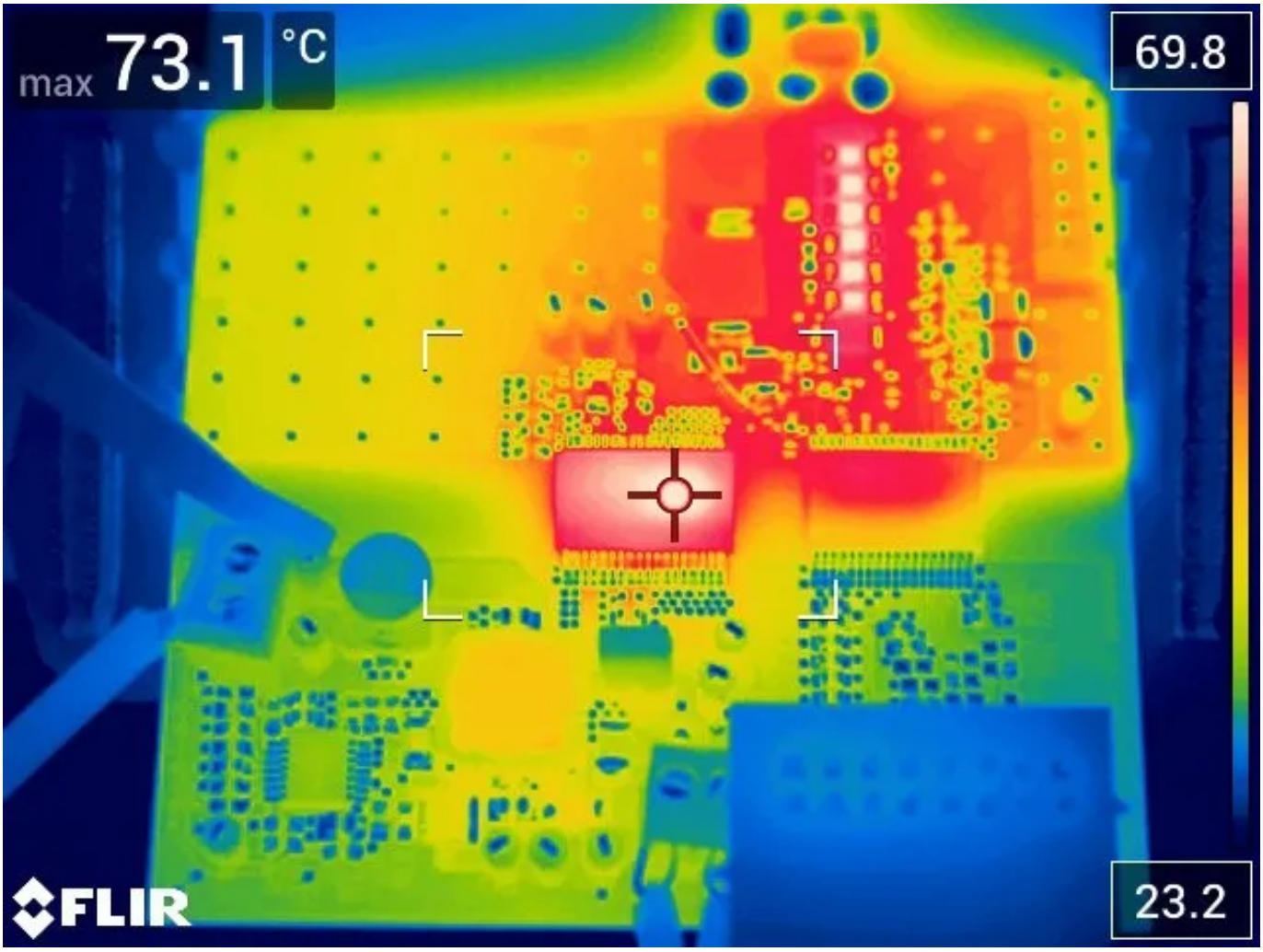

Figure 5. Automotive SPI-programmable reference design thermal image with 1.6-W loading. Source: Texas Instruments

These two approaches make providing isolated power for gate drives in high-power inverters and battery chargers much less of a design challenge, with the added bonus of also reducing radio-frequency noise at the system level. The first approach enables multiple isolated outputs controlled by a single IC. With the second approach, one IC with only filter capacitors and divider resistors provides a complete isolated power solution.

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Technical Article

How to reduce the THD of a PFC

Bosheng Sun

Total harmonic distortion (THD) is the harmonic distortion present in a signal, defined as the ratio of the root-mean-square (RMS) amplitude of a set of higher harmonic frequencies to the RMS amplitude of the first harmonic, or fundamental frequency. Equation 1 expresses THD:

$$THD = \frac{\sqrt{V_2{}^2 + V_3{}^2 + V_4{}^2 + \cdots}}{V_1} \quad (1)$$

where V_n is the RMS value of the nth harmonic and V_1 is the RMS value of the fundamental component.

In power systems, these harmonics can cause problems ranging from telephone transmission interference to conductor degradation; therefore, it is important to control the total THD. A lower THD means a lower peak current, less heating, lower electromagnetic emissions, and less core loss in motors.

Reducing THD needs power factor correction (PFC), which is required for AC/DC power supplies that have input power greater than 75 W. PFC forces the input current to follow the input voltage such that the electronics load draws a sinusoidal current waveform that contains minimal harmonics.

THD requirements have become stricter, especially in server applications. The Modular Hardware System-Common Redundant Power Supply (M-CRPS) specification defines a very strict THD requirement across the entire load range, as shown in Table 1. This is much stricter than the previous CRPS THD specification.

Table 1. The M-CRPS THD specification. Source: Texas Instruments

Output power	< 5%	5%≤In≤10%	10%<Iin≤20%	20%<Iin≤50%	50%<Iin≤100%
Current iTHD (240VAC) Capacity Levels ≥ 1400W	< 20%	< 8.5%	< 7.5%	< 5%	< 3.5%
Current iTHD (240VAC) Capacity Levels < 1400W	< 25%	< 10%	< 10%	< 7.5%	< 4%
Current iTHD (120VAC)	< 25%	< 10%	< 7.5%	< 5%	< 4%

Meeting such strict THD specifications is a big challenge in PFC designs where traditional loop tuning may not be enough. In this article, I'll suggest a few extra methods to help reduce THD.

Make sure that the sensed signals are clean

The PFC controller senses the AC input voltage, inductor current and PFC output voltage. These sensed signals need to be clean; otherwise, they will affect THD. For example, because the AC input voltage signal generates a sinusoidal current reference, any spikes on the sensed signal will cause current reference distortion and affect THD.

Although the output voltage (V_{OUT}) signal is not used for generating a current reference, it can affect THD because the spikes on V_{OUT} will cause a ripple on the voltage-loop output, which affects the current-loop reference and eventually THD. If the spike's magnitude is large enough, it may trigger a voltage-loop nonlinear gain, significantly raising THD.

One common practice is to put a decoupling capacitor close to the sense pin of the controller. You will have to carefully select the capacitance such that it will effectively reduce the noise but not cause too much delay. Using

a digital infinite impulse response filter to process the sensed V_{OUT} signal will further reduce the noise; because the PFC voltage loop is slow, the extra delay caused by this digital filter is acceptable.

For AC voltage sensing, however, it is not recommended to add a digital filter because it will cause a delay on the current reference. In this case, you can use a firmware phase-locked loop (PLL) to generate an internal sine wave signal in phase with the AC voltage, and then use that generated sine-wave signal to modulate the current reference. Since the PLL-generated sine wave is clean, even if there is some noise on the sensed AC voltage, the current-loop reference will also be clean.

Reduce the current spikes at AC zero crossing

Current spikes at AC zero crossing are an inherent issue for the totem-pole bridgeless PFC. These spikes can be so big that it becomes impossible to pass M-CRPS THD specifications. I've analyzed the root cause of these spikes, and noted that a pulse-width modulation (PWM) soft-start algorithm, as shown in Figure 1, will effectively reduce them.

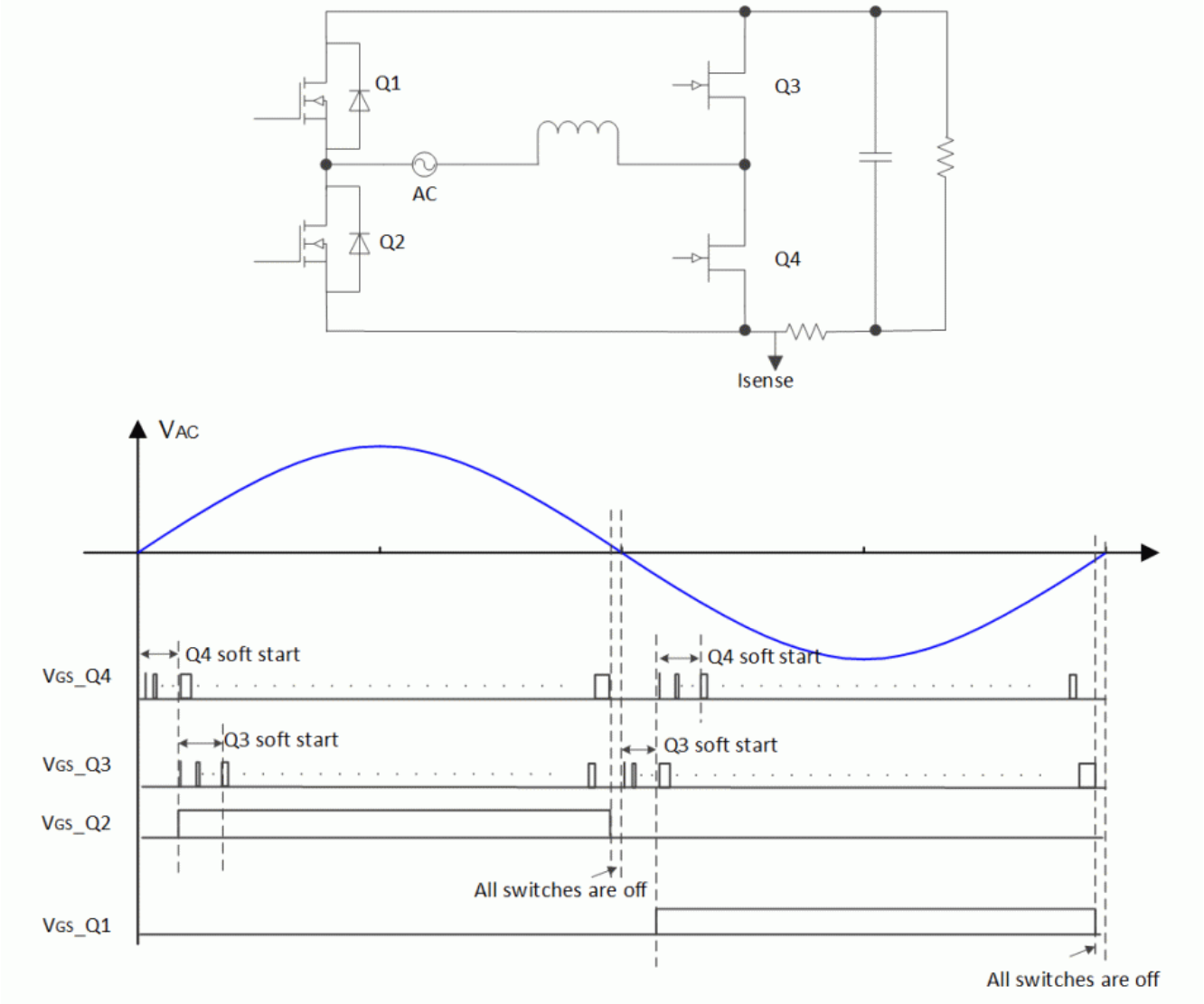

Figure 1. Gate signal timing for AC zero crossing. Source: Texas Instruments

In this solution, when V_{AC} changes from a negative to a positive cycle after AC zero crossing, active switch Q4 turns on first with a very small pulse width, then gradually increases to the duty cycle (D) generated by the control loop. A soft start on Q4 gradually discharges the switch-node drain-to-source voltage (V_{DS}) to zero.

Once Q4's soft start is complete, synchronous transistor Q3 starts to turn on. It begins with a tiny pulse width and gradually increases until the pulse width reaches 1-D. When Q4's soft start is complete and Q3's soft start begins, the low-frequency switch Q2 turns on.

The zero-crossing detection could be undesirably triggered by noise. For safety purposes, at the end of the half AC cycle, turn off all of the switches. This leaves a small dead zone that will prevent the input AC from short-circuiting. The transition from the AC positive cycle to the negative cycle is the same. Figure 2 shows the test result.

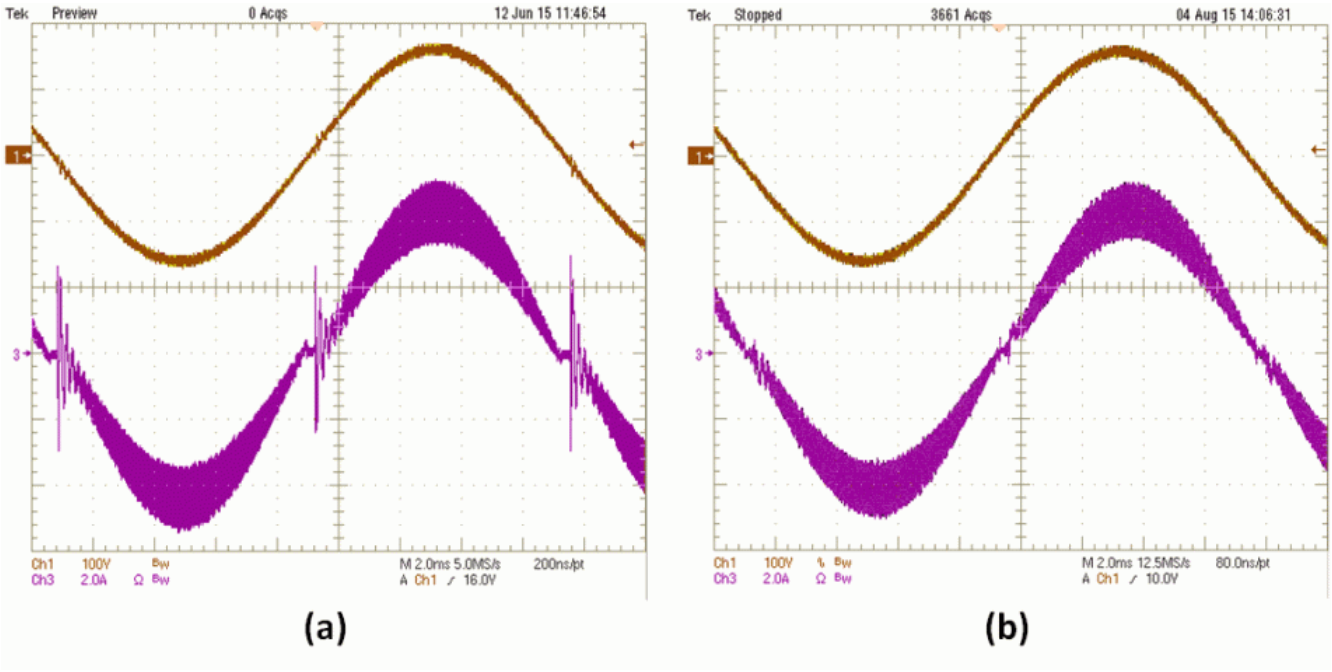

Figure 2. Current waveforms without and with a PWM soft start: the traditional control method (a) and PWM soft start (b). Source: Texas Instruments

Reduce voltage-loop effects

The double-line frequency ripple on the voltage-loop output can affect the current reference and thus THD. To reduce this frequency ripple effect as much as possible - while at the same time not sacrificing the load transient response - you could add a digital notch (band-stop) filter between the V_{OUT} sensed signal and the voltage loop. This notch filter can effectively attenuate the double-line frequency ripple while still passing all other frequency signals, including the sudden V_{OUT} change caused by the load transient. The load transient will not be affected.

Another approach is to sense V_{OUT} at the AC zero-crossing instance. Since the V_{OUT} value at AC zero-crossing instance Vout_zc(t) equals its average value and it is a "constant" in steady-state, it is the perfect feedback signal for voltage-loop control. To handle the load transient, use this voltage-loop control law:

```
If ((Vref – Vout(t) < Threshold)
{
Error = Vref – Vout_zc(t);
VoltageLoop_output = Gv(Error, Kp, Ki);
}
Else
{
Error = Vref – Vout(t);
```

VoltageLoop_output = Gv(Error, Kp_nl, Ki_nl);

}

If the instantaneous V_{OUT} error is small, use the V_{OUT} value at the AC zero-crossing instance Vout_zc(t) and small proportional-integral (PI) loop gain Kp, Ki for voltage-loop compensator Gv. When a load transient occurs causing an instantaneous V_{OUT} error greater than the threshold, use the instantaneous Vout(t) value and PI loop gain Kp_nl, Ki_nl for Gv to rapidly bring V_{OUT} back to its nominal value.

Oversampling

The PFC inductor current is a saw wave with DC offset in each switching cycle; the current then goes to a signal-conditioning circuit such as an operational amplifier to make the signal suitable for the PFC control circuit. However, this signal-conditioning circuit does not provide sufficient attenuation to the input current ripple. The current ripple still appears at the output of the amplifier. If this signal is sampled only once in each switching period, there is no perfect, fixed location where the signal represents the average current all of the time. Thus, with a single sample, it is very difficult to achieve good THD.

To get a more accurate feedback signal, I recommend an oversampling mechanism. Figure 3 shows that it is possible to evenly sample the current feedback signal eight times in every switching cycle, average the results, and send them to the control loop. This oversampling effectively averages the current ripple out such that the measured current signal gets closer to the average current value. Also, the controller becomes less sensitive to noise - both signal noise and measurement noise. Oversampling is one of the most effective ways to reduce current waveform distortions.

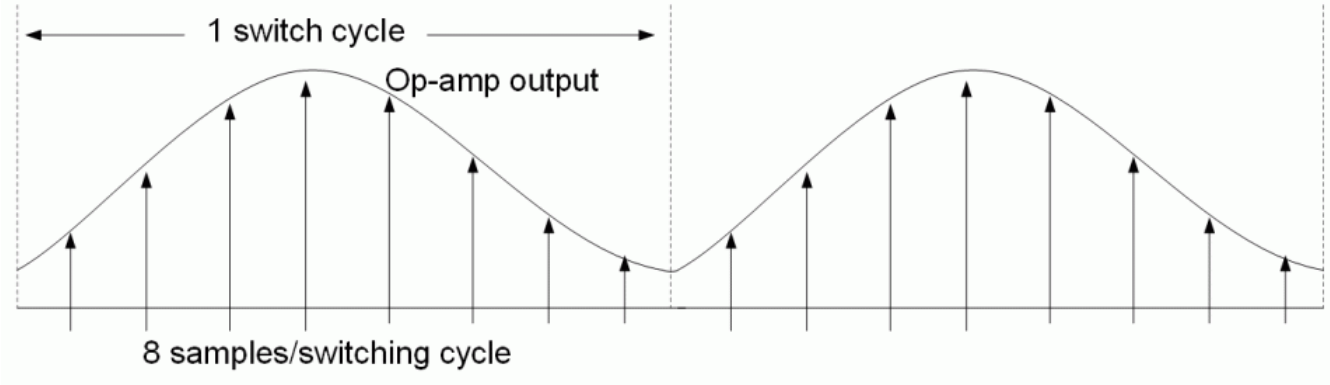

Figure 3. Oversampling eight times in every switching cycle. Source: Texas Instruments

Duty-ratio feedforward

The basic idea of duty-ratio feedforward control is to pre-calculate a duty ratio, then add this duty ratio to the feedback controller. For a boost topology operating in continuous conduction mode, Equation 2 gives the duty ratio (d_{FF}) as:

$$d_{ff} = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (2)$$

This duty-ratio pattern effectively produces a voltage across the switch whose average over a switching cycle is equal to the rectified input voltage. A regular current-loop compensator changes the duty ratio around this calculated duty-ratio pattern.

Figure 4 depicts the resulting control scheme. After using Equation 2 to calculate d_{FF}, it is then added to the traditional average current-mode control output (d_I). You could then use the final duty ratio (d) to generate a PWM waveform to control PFC.

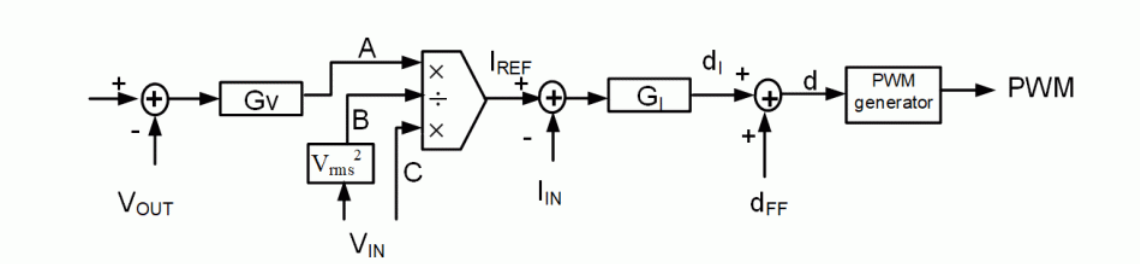

Figure 4. Average current-mode control with d_{FF}. Source: Texas Instruments

Since the majority of the duty cycle is generated by duty-ratio feedforward, the control loop only adjusts the calculated duty slightly. This technique can help improve THD for applications with a limited controller loop bandwidth.

AC cycle skipping

In general, it's harder to meet light-load THD requirements than heavy-load THD requirements; this is especially true for the 5% load THD requirement in the M-CRPS specification. If the PFC meets all other THD requirements except at a 5% load, even if you have tried all the methods mentioned so far, an AC cycle-skipping method can help.

Think of AC cycle skipping as a special burst mode: when the load is less than a pre-defined threshold, the PFC enters this mode and, depending on the load, skips one or more AC cycles. In other words, the PFC turns off for one or more AC cycles and turns back on for the next AC cycle. The turnon and turnoff instance is at the AC zero crossing such that the whole AC cycle is skipped. Since PFC turnon and turnoff at current equal zero, there is less stress and electromagnetic interference. AC cycle skipping is different than the traditional PWM pulse-skipping burst mode, where you skip PWM pulses randomly.

The number of AC cycles to skip is reverse-proportional to the load; the less load, the more AC cycles skipped. Figure 5 shows the skipping of one AC cycle. Channel 1 is the AC voltage, and channel 4 is the AC current.

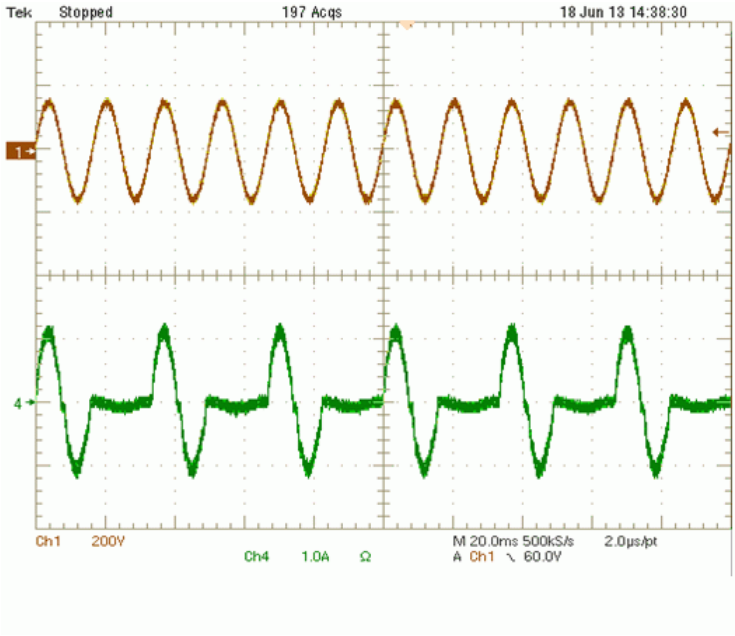

Figure 5. AC cycle skipping at a light load. Source: Texas Instruments

When the PFC turns off because the current is zero, THD is zero. Since the PFC needs to compensate for the turnoff period, it delivers a large amount of power when it turns on, which is greater than the average value.

Essentially, this operates the PFC either at medium load, or it completely turns off. Since THD is much lower at a middle load than at a light load, light-load THD is reduced.

Test results

I implemented the methods described in this article on a 3-kW totem-pole bridgeless PFC [5] controlled by a Texas Instruments C2000™ microcontroller. Figure 6 shows the THD test result at 240 V_{AC}.

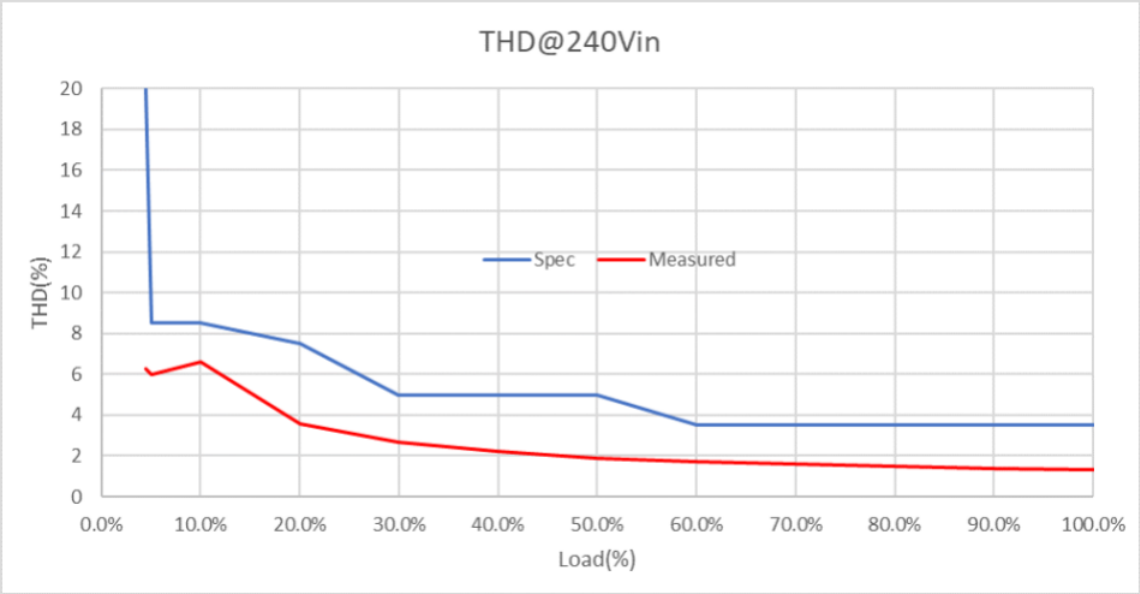

Figure 6. THD test results. Source: Texas Instruments

The THD not only meets the latest M-CRPS THD specifications but also has plenty of margin, which guarantees that the PFC will meet specifications during mass production, even with hardware tolerance.

Related Content

- Power Tips #115: How GaN switch integration enables low THD and high efficiency in PFC
- Power Tips #114: A potential firmware mistake may lead to control instability
- Power Tips #113: Two simple isolated power options for 8 W or less
- Power Tips #112: Onboard fixtures for fault testing

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4. Sun, Bosheng. “AC Cycle Skipping Improves PFC Light-Load Efficiency.” Texas Instruments Analog Design Journal article, literature No. SLYT585, 3Q 2014.
5. Texas Instruments. n.d. “3-kW, 180-W/in3 Single-Phase Totem-Pole Bridgeless PFC Reference Design with 16-A Max Input.” Texas Instruments reference design No. PMP23069. Accessed April 10, 2023.

Technical Article

Load transient testing with high slew rates

Robert Taylor

Microprocessors and application-specific integrated circuits (ASICs) require low-voltage, high-current power supplies. These supplies usually have very strict requirements on output-voltage deviations, especially to load transient events. Testing these supplies can pose a challenge for designers, and it may be difficult to confirm compliance with the specifications.

In Power Tip 63, Robert Kollman covered some of the issues associated with load transient testing. Here, I will cover additional details as well as methods that you can use to simplify testing of these difficult conditions.

First, you need to understand all of the transient specifications in order to properly design the supply, while also understanding how they apply to the testing. Typical transient specifications include:

- The size of the load step in amperes or given as a percentage of the full load.
- The minimum load during a transient event (sometimes zero).
- The slew rate of the load step, usually in amperes per microsecond.
- The maximum voltage deviation allowed on both edges of the step.
- The expected recovery time.

Figure 1 shows an example of how these specifications are usually defined.

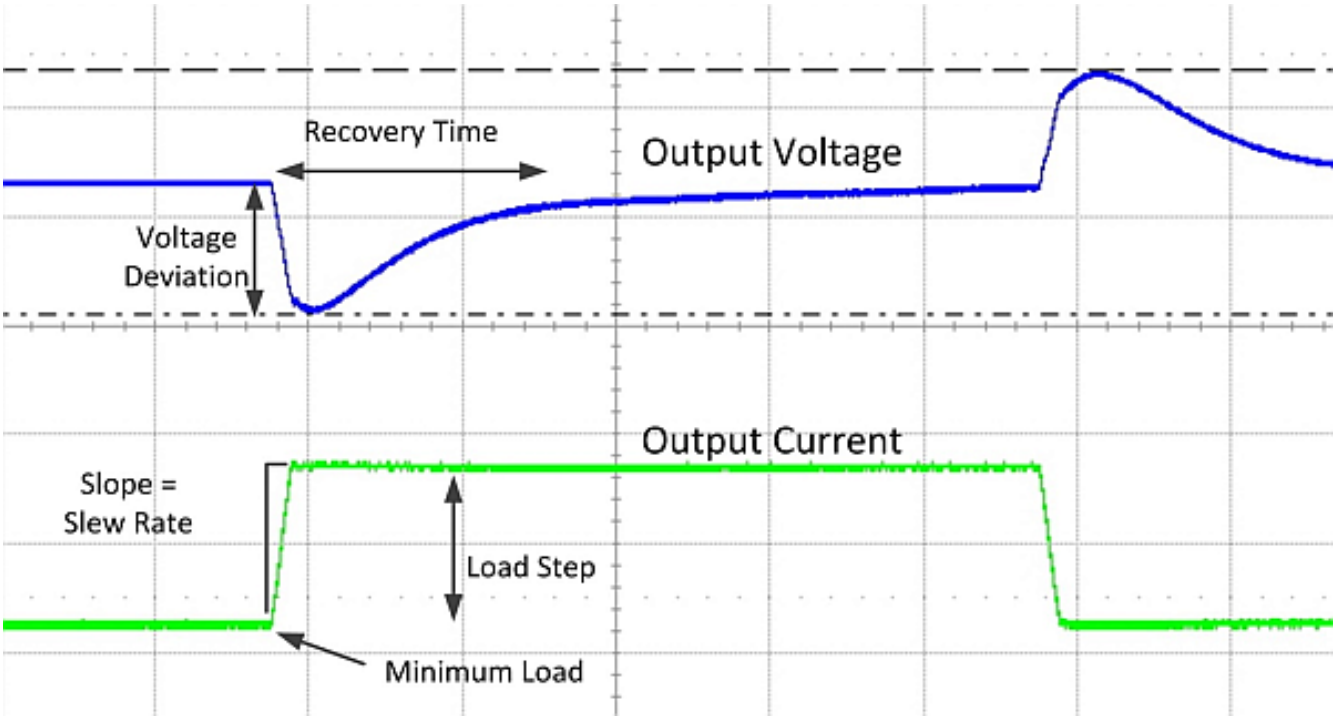

Figure 1. Graphical description of a load transient measurement

Once you understand all of the specifications, you can attempt to design the supply to meet the requirements. Testing said requirements then becomes the challenge, however. It is not unusual to see requirements for an output voltage of 1V, a load step of 100A and a slew rate of 1,000A/µs. The limiting factor in most testing situations is the inductance between the power supply under test and the load. In a real system, the power supply is often right next to the load it is powering; thus the parasitic inductance is minimized.

You can use a number of methods to test the load transient response for a given power supply; each has its pros and cons. Here, I'll compare the following options: an external electronic load, an external transient board, a "field-effect transistor (FET) slammer," an onboard transient generator and a socket-based transient tester.

The external electronic load is probably the most common method for testing transient response – and the most convenient. Most loads have modes that enable you to easily set the current levels and transition times. The main drawback is limited slew rate, either caused by external wiring or limitations of the actual load.

An external transient board can usually achieve better results in terms of slew rate, but at the cost of flexibility. Depending on the design, the load transient board may be limited in maximum current, thermal dissipation or slew rate. Because the transient board is connected externally, wiring is often the slew-rate-limiting bottleneck. Also, you need to adjust or configure the board for each power supply that you test.

A FET slammer is a quick and crude method for getting high-speed transient results. You connect a metal-oxide semiconductor field-effect transistor (MOSFET) from drain to source through a resistor or directly across the output of the power supply; a function generator controls the gate. Because there is minimal external wiring, there's a major reduction in parasitic inductance.

While this method can usually generate a high slew rate, the control and repeatability of the testing may be difficult. You may also have to modify the printed circuit board (PCB) (Figure 2). Another issue with this method is that measuring the actual load step current is difficult and can be inaccurate.

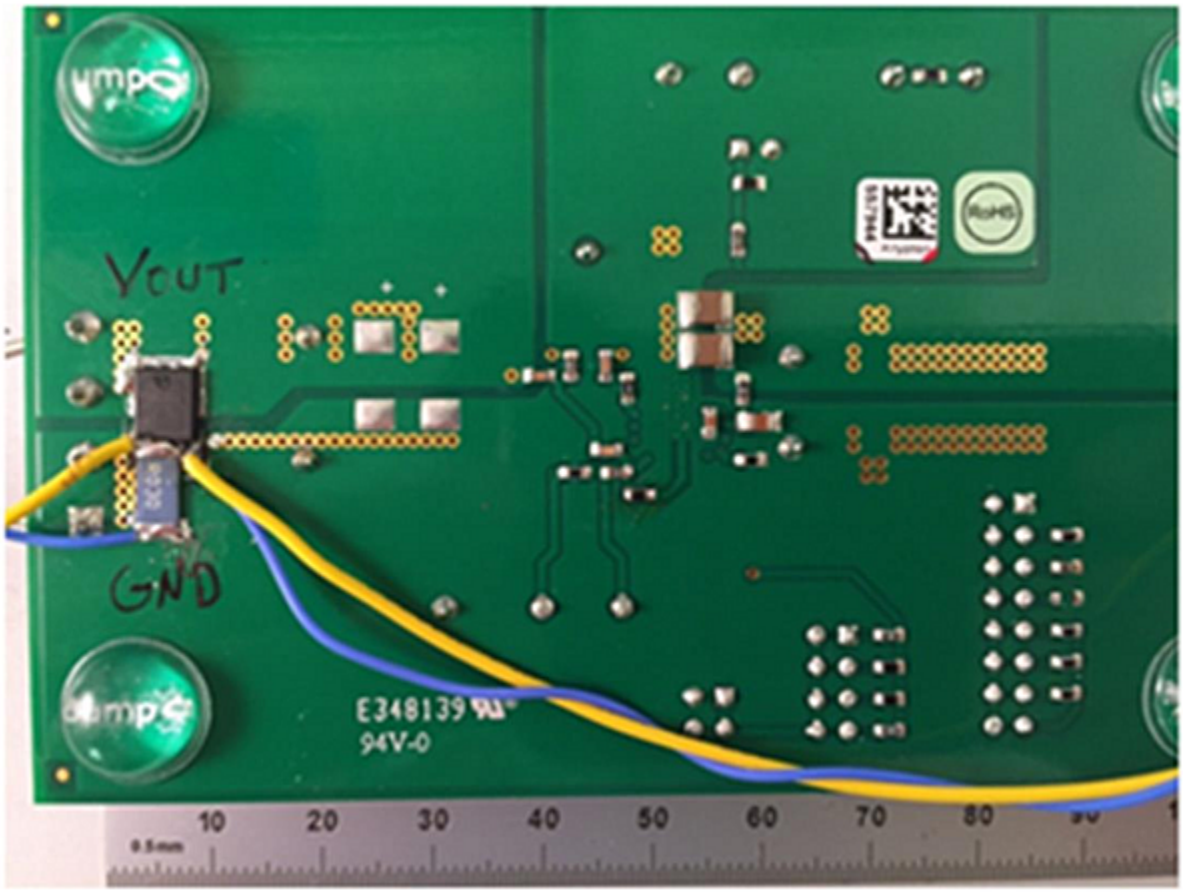

Figure 2. Example of a PCB with a FET slammer

Onboard transient generators can be very helpful when trying to test the performance of high-current high-speed transients. You can design the circuit for the exact load transient specification. The main drawbacks are extra cost and space taken by the components. In addition, the flexibility to take multiple different measurements might be difficult or time-consuming.

The design of an onboard transient generator can be quite complex as well. It can be as simple as a resistor and FET controlled by a 555 timer or as complicated as something like what's shown in Figure 3. The more complex design uses multiple stages and smaller, faster-switching FETs. This type of design can achieve slew rates of 1,000A/µs.

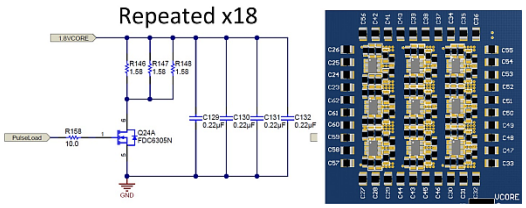

Figure 3. A more complex version of an onboard transient generator

The final option is to use a processor socket and a specialized transient tester tool. This option is the most expensive route, as the tool itself can be expensive and the PCBs become much more costly. However, you may achieve the most accurate results for a given set of processor requirements. The processor or ASIC manufacturer often develops these tools, so they are built specifically to deliver the right test conditions.

Table 1 summarizes the transient testing options.

Table 1. Comparison of different transient testing methods

Method	Pros	Cons
External electronic load	Simple, flexible, possibly no extra cost	Limited slew rate due to external connections
External transient board	Simple, low cost	Needs to be modified for each test; limited slew rate due to external connections
FET slammer	Low cost, fast slew rates	Requires a fancy function generator; measuring the actual current can be difficult and inaccurate; possibly hard to control
Onboard transient generator	Very fast slew rates; designed specifically for the supply under test	Each different test condition requires modifications to the board; takes up extra space on the PCB; could add cost; difficult to measure current
Socket-based transient tester	Very specific testing for exact compliance; generally controlled through software to make testing easy	Very expensive; difficult PCB layout to accommodate socket; PCBs can be very expensive because of layer count and socket placement

Testing for load transients is a very important part of power-supply design and compliance. Parasitic inductance in test fixtures can negatively impact your ability to achieve the desired slew rates. Using the methods I've described here, I hope you can avoid this problem.

To learn more about transient loads, read the Power House blog: Power Tips: A Simple Circuit Yields Fast, Controllable Transient Loads.

For more Power Tips, check out TI's Power Tips blog series.

Also see:

- Testing a power supply
- Load-transient-response testing for voltage regulators
- Power Tip 63: Testing High-di/dt Power Supplies
- Power Tips #78: Synchronous rectifiers improve cross-regulation in flyback power supplies
- Power driver design handles difficult loads, helps characterize PSUs
- Power transient buffer enables IC & circuit testing
- Transient load gives power systems a workout

Technical Article

Measure your LLC resonant tank before testing at full operating conditions

John Dorosa

Half-bridge series resonant converters achieve high efficiencies and high power densities for converters over 100 W. The most common resonant topology (Figure 1) is a resonant tank comprising of a series magnetizing inductor, resonant inductor and a capacitor (abbreviated as LLC). The selection of parameter values determines the shape of the resonant tank's gain curve, which affects how the resonant converter performs in a system.

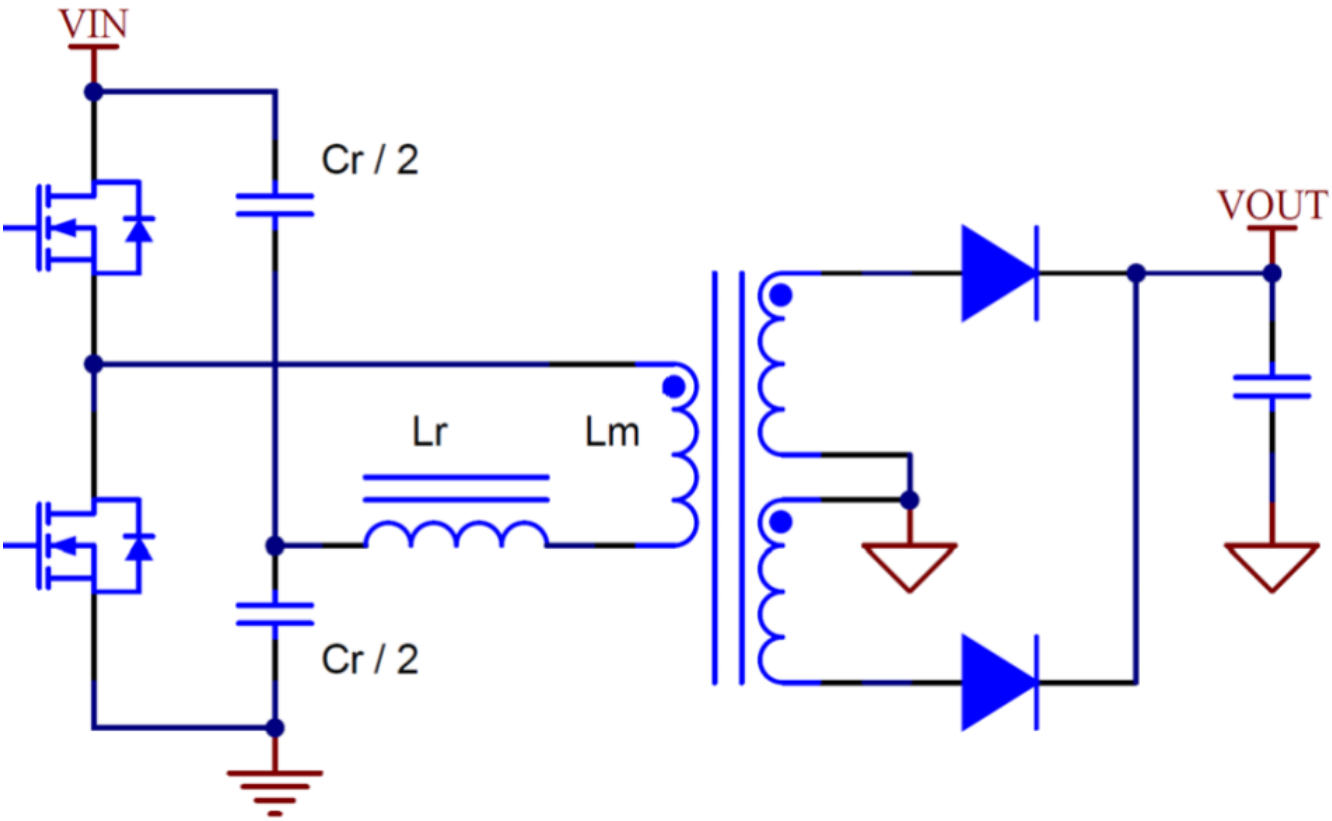

Figure 1. A half-bridge LLC power stage with split resonant capacitors, the selection of parameter values determines the shape of the resonant tank's gain curve which needs to be verified before applying energy to the circuit. Source: Texas Instruments

Once you have settled on a set of parameters and selected the components, it is very important to verify the gain curve before applying energy to the circuit. In this power tip I will describe a technique for measuring a resonant tank's gain curve and how to interpret the results, including examples that show both the strengths and limitations of this technique.

A frequency response analyzer injects a small AC signal to any circuit, then measures the voltages at two points in the system to determine the signal gain and phase delay across a determined frequency range. While this equipment is most commonly used for testing a control loop, you can also use a frequency response analyzer to measure the gain of the power stage of an LLC converter. Figure 2 shows the wiring diagram for such a measurement.

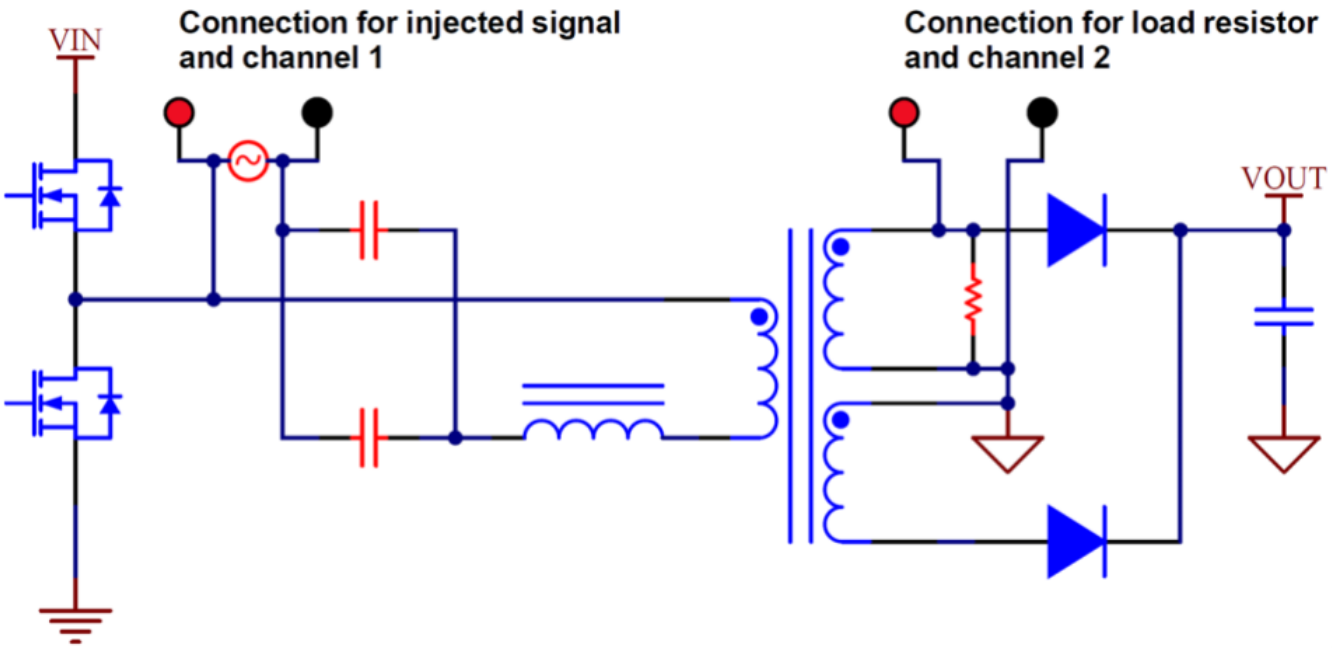

Figure 2. Wiring diagram for connecting a resonant tank to a frequency response analyzer to recreate gain curve plots. The gain plot of the power stage can be obtained by displaying the magnitude of channel 2's voltage divided by channel 1's voltage. Source: Texas Instruments

The half-bridge LLC has a pair of resonant capacitors, with one tied to the input voltage and the other tied to primary ground. To run the test in this circuit, the resonant capacitors must be in parallel with each other and in series with the primary winding. The injection signal and channel 1 measurement of the analyzer connect across the primary-side components from the switching node of the half bridge to the other end of the resonant capacitors. The secondary channel of the analyzer, channel 2, connects across the secondary winding, with a resistor added to approximate the loading conditions. After sweeping the frequency of the injected AC signal, you can plot the gain of the power stage by displaying the magnitude of channel 2's voltage divided by channel 1's voltage. Figure 3 shows an example test result.

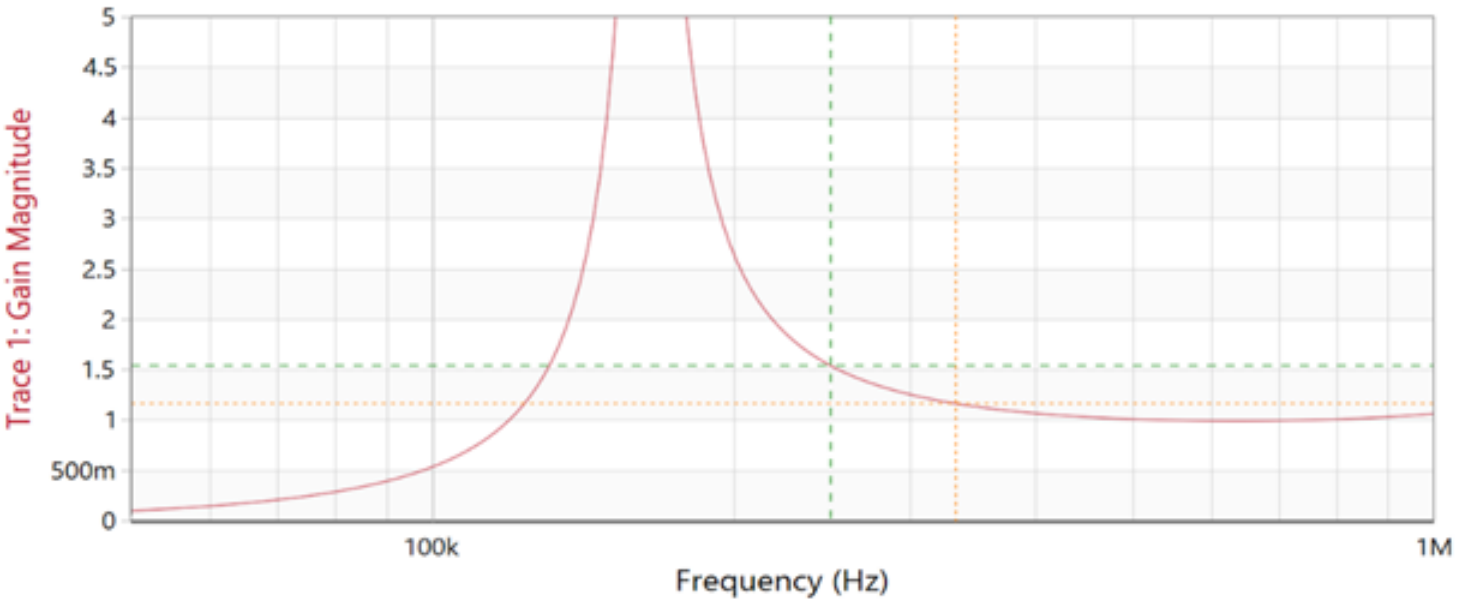

Figure 3. A sample LLC resonant tank gain curve measurement that can be observed from the test setup shown in Figure 2. Source: Texas Instruments

You can convert the power-stage gain to a voltage gain depending on the transformer turns ratio and the configuration of switches and windings on the primary and secondary sides of the power stage. A half-bridge LLC power stage is typically shown with a center-tapped secondary winding and two output rectifiers. In this example, the output voltage is approximately the product of the input voltage, turns ratio and gain of the resonant tank at the operating frequency. Other options for secondary configurations drawn in Figure 4 enable the resonant tank to convert to higher output voltages. Note that if the primary side is configured with a full bridge, you will need to multiply these ratios by a factor of two.

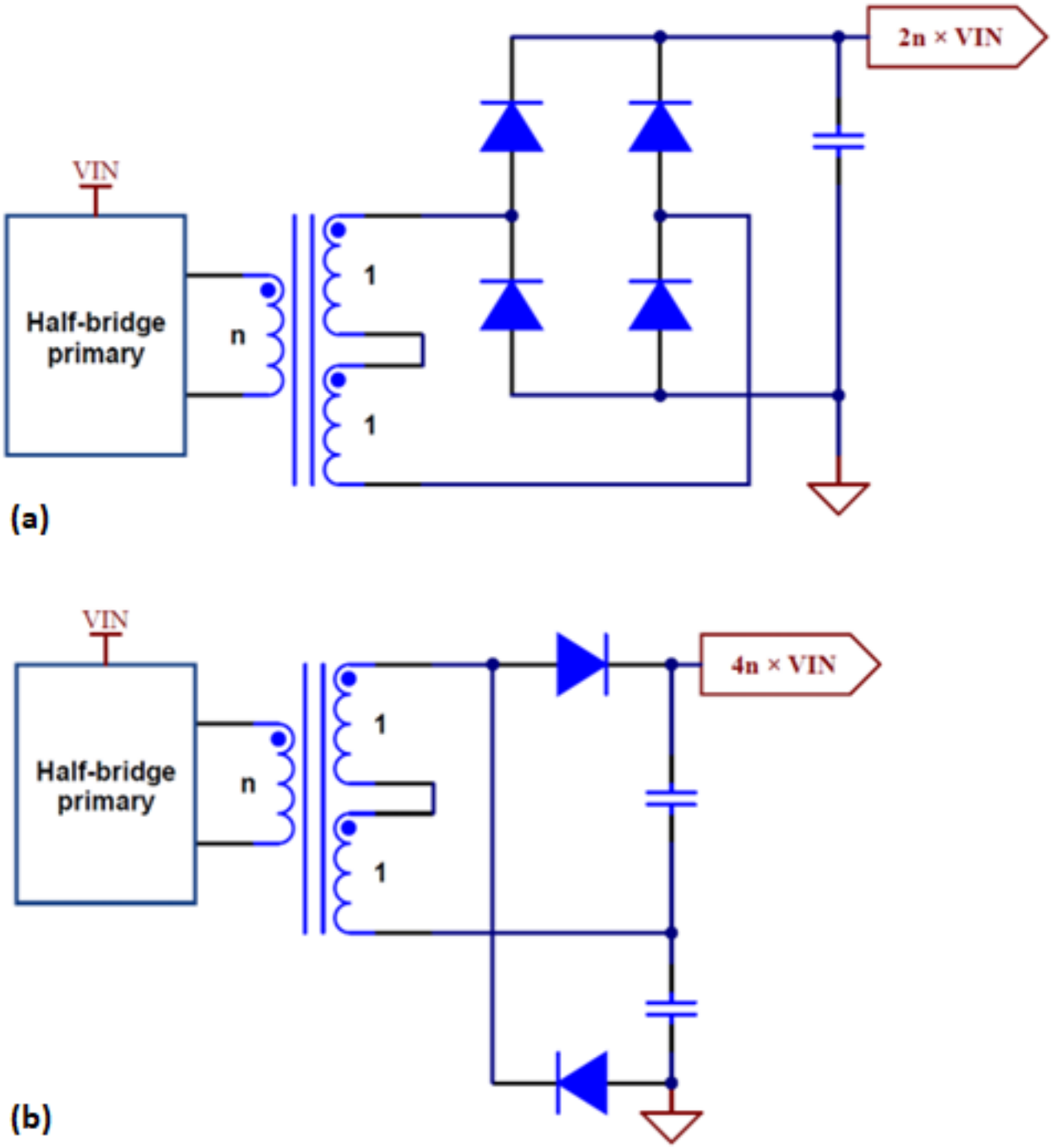

Figure 4. Configuring the secondary-side with a full-wave rectifier doubles the transferred energy (a); a double-ended secondary configuration achieves a fourfold voltage gain (b). Source: Texas Instruments

A benefit to this technique is that you can take the measurement directly on the PCB and account for power-stage parasitic elements in the test results. The TI E2E™ design support forums article, "Why is Your LLC Resonant Converter Frequency Way, Way Off," uses an alternate model to explain how the construction of the transformer introduces additional inductances into the circuit (Figure 5). You can design around these inherent parasitic components or integrate them into your design. For example, you can use the leakage inductance as the resonant inductor, which saves cost and improves efficiency by removing a physical component from the design. It's possible to simplify the optimization of a resonant tank design with this method by using this quick test.

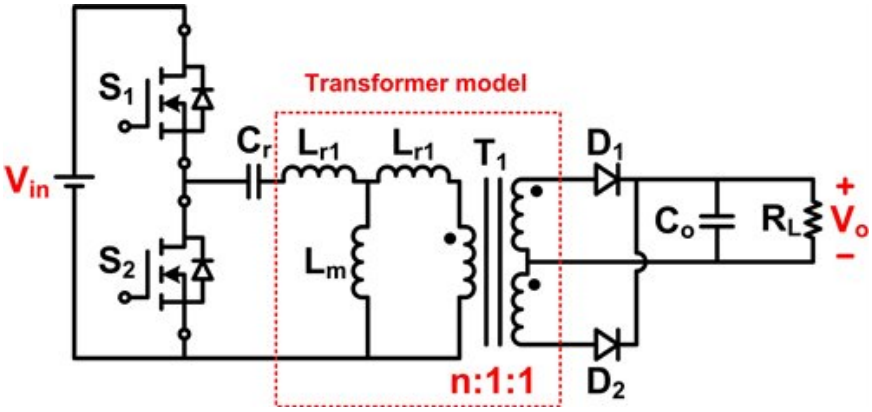

Figure 5. Transformer model using leakage inductance as a resonant element for an LLC converter, allowing designers to either design around inherent parasitic components or integrate them into the design. Source: Texas Instruments

Using synchronous rectifiers on the secondary will further improve the LLC converter efficiency. Doing so will lower conduction losses, which tend to dominate the total loss characteristic for that component; however, the choice of MOSFETs can change the shape of the gain curve. Lower-resistance MOSFETs will have a larger output capacitance. The turns ratio of the transformer can amplify this capacitance, which can then become an issue in some cases. As I mentioned, testing the gain curve in circuit helps account for additional parasitic elements throughout the power stage. Figure 6 highlights the effects of MOSFET output capacitance that may have gone unnoticed in the initial resonant tank design.

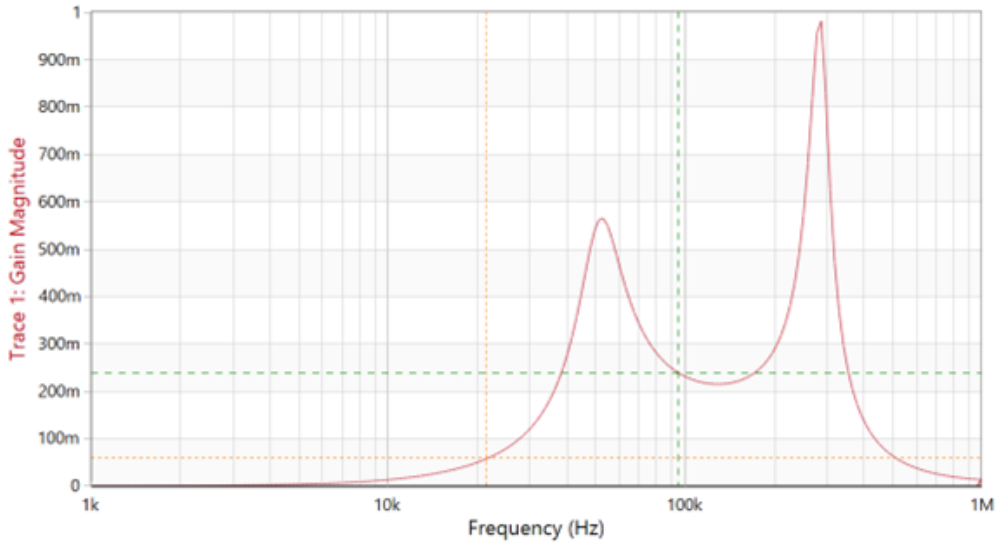

Figure 6. In this design, parasitic capacitance added a resonance at around 300 kHz that was not intended to be there in the design phase. Source: Texas Instruments

However, using a frequency response analyzer cannot account for all design parasitic elements. For example, the measurement will not show the effects of secondary windings that are not well-coupled to each other on a center-tap structure. Loose couplings between the primary and secondary windings will form leakage inductance, and this is beneficial to an extent in LLC designs. Secondary windings that are not well-coupled to each other will decrease the performance of the power stage, however. It is not possible to observe the effects of this in AC analysis, but it will be apparent when monitoring the secondary winding voltages.

For example, the design in Figure 7 had a correct gain curve. But when looking at the voltage across the secondary windings, the level started out higher and drooped to a level lower than the output voltage. Ideally, these voltage waveforms should look more like a square wave. Loose coupling also creates a large leakage spike on the secondary rectifier turnoff edge. As the load increases, the distorted effects of the secondaries loosely coupled to each other become more noticeable and limit the possible output. power.

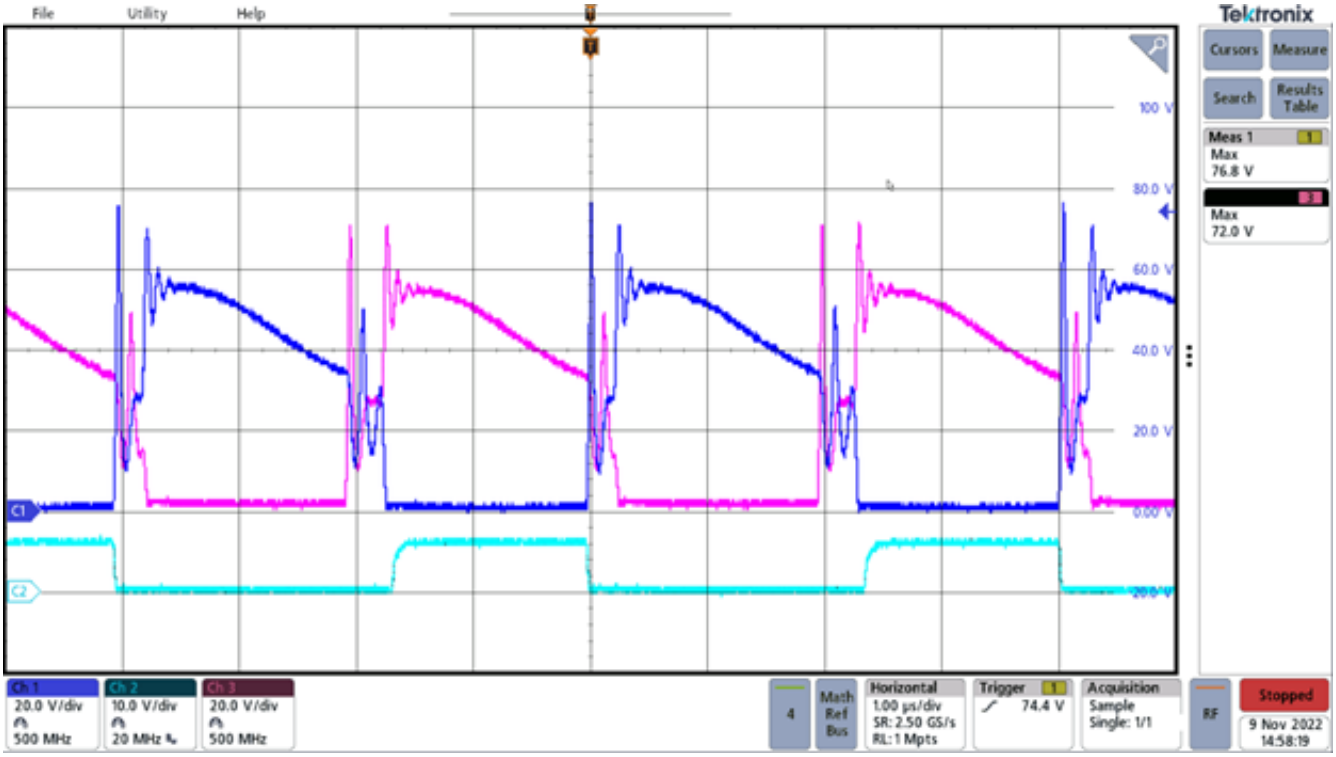

Figure 7. The loose coupling in a transformer design is noticeable in switching waveforms but was not apparent in its gain curve. Source: Texas Instruments

Even after reconfiguring this transformer design to have the secondary windings better coupled to each other, the resulting resonant inductance and magnetizing inductance remained the same. There was no visual difference in the gain curve measurements, as expected. But the switching waveforms in Figure 8 illustrated a noticeable improvement with the new design.

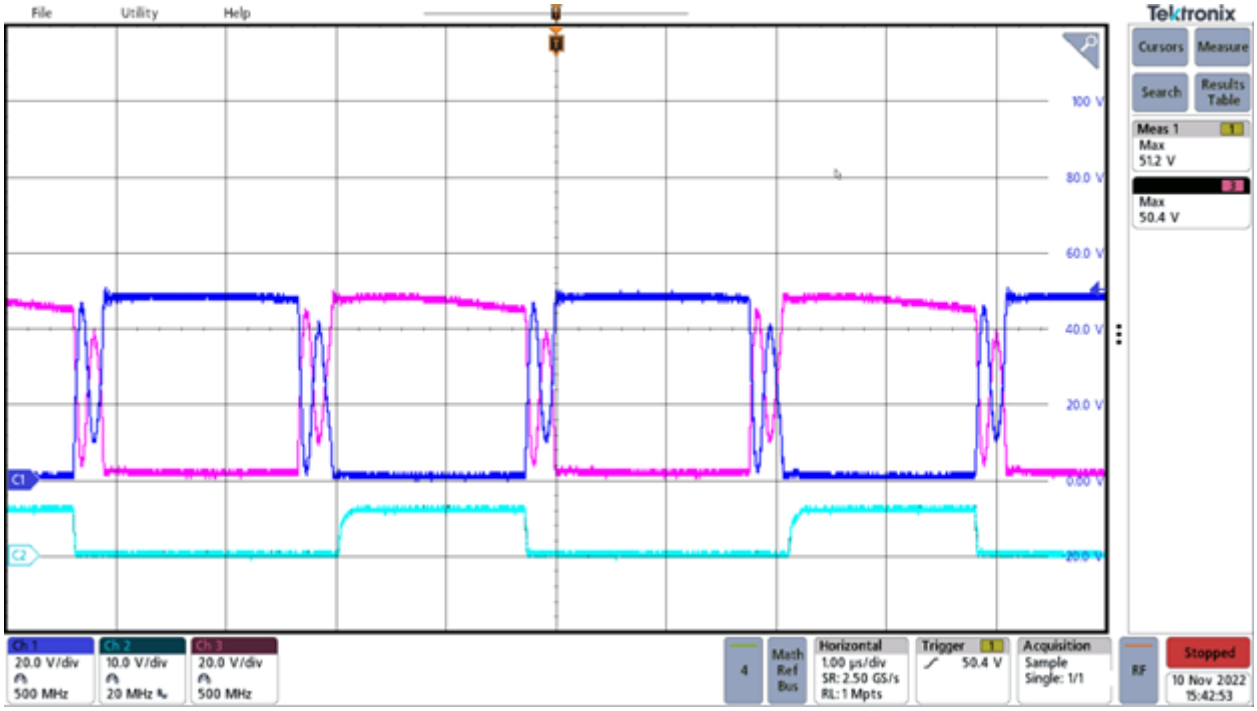

Figure 8. An improved transformer design with better coupling mitigated voltage droop while maintaining the gain curve shape. Source: Texas Instruments

With the secondary windings reconfigured, the switching waveforms look closer to expectations; the waveform is more square-shaped, with the blocking voltage equal to the output voltage. The leakage spike by the turnoff edge was also eliminated.

The two transformer designs were effectively the same, requiring no additional components. Yet the changes had a large impact on overall efficiency.

When designing a resonant converter, start your evaluation by validating the gain curve of the resonant tank. While it cannot detect all faults, you will get some insight into the achievable gain, as well as the expected operating frequency range.

Related Content

- Power Tip #84 Think outside the LLC series resonant converter box
- Power Tips #103: LLC design considerations for audio amplifiers
- Power Tips #89: High-frequency resonant converter design considerations, Part 1
- Power Tips #92: High-frequency resonant converter design considerations, Part 2
- Power Tips #97: Shape an LLC-SRC gain curve to meet battery charger needs

Additional resources

- Power Tips: Get to know LLC series resonant converter design
- Power Tips: How much can a LLC series resonant converter do?
- Power Tips: Designing an LLC resonant half-bridge power converter

Technical Article

How GaN switch integration enables low THD and high efficiency in PFC

Brent McDonald

The need for cost-effective solutions to improve power factor correction (PFC) at light loads and with peak efficiency while shrinking passive components is becoming difficult with conventional continuous conduction mode (CCM) control. Engineers are conducting significant research into complex multimode solutions to address these concerns [1], [2], and these approaches are attractive in that they enable you to shrink the size of the inductor while simultaneously improving efficiency with soft switching at lighter loads.

But in this power tip, I will present a new approach to achieving high efficiency and low total harmonic distortion (THD) that does not require the use of a complex multimode control algorithm and achieves zero switching losses under all operating conditions. This approach uses a high-performance gallium-nitride (GaN) switch with an integrated flag that indicates whether the switch turns on with zero voltage switching (ZVS). This approach enables high-efficiency ZVS under all operating conditions while simultaneously forcing the THD very low.

Topology

The topology used for this system is the integrated triangular current mode (iTCM) totem-pole PFC [3]. For high-power and high-efficiency systems, the totem-pole PFC offers a distinct advantage for conduction losses. The TCM version of this topology enforces ZVS by making sure that the inductor current always goes sufficiently negative before the switch turns on [4]. Figure 1 illustrates the iTCM version of totem-pole PFC.

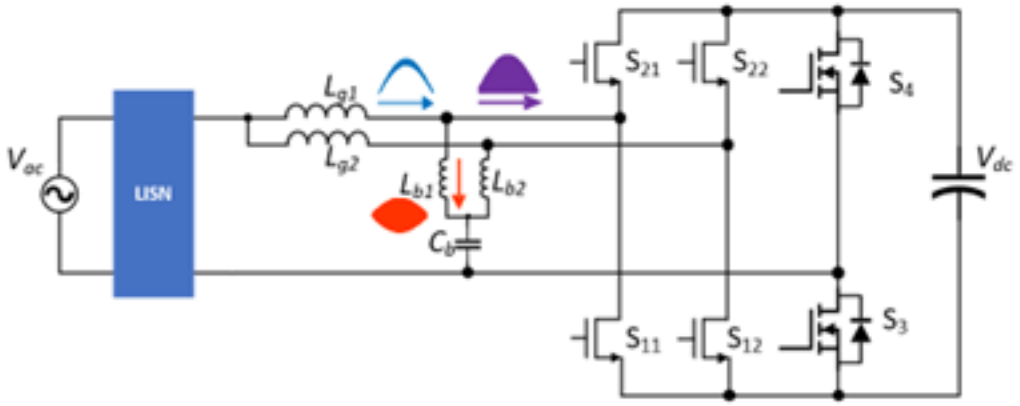

Figure 1. The iTCM topology, showing AC line frequency current envelopes.

The difference between the TCM converter and the iTCM converter is the presence of L_{b1}, L_{b2} and C_b. During normal operation, the voltage across C_b is equal to the input voltage V_{ac}. Two phases operating 180 degrees out of phase take advantage of ripple current cancellation and reduce the root-mean-square current stress in C_b. L_{b1} and L_{b2} are sized to only process the high-frequency AC ripple current necessary for TCM operation. This removes the DC bias required for the inductor used in TCM, as defined in [4]. Ferrite cores for L_{b1} and L_{b2} help ensure low losses in the presence of the high flux swings necessary for ZVS. L_{g1} and L_{g2} are larger in value (as much as 10 times larger) than L_{b1} and L_{b2}, which prevents most of the high-frequency current from flowing into the input source and subsequently reduces electromagnetic interference (EMI). In addition, the reduced ripple current in L_{g1} and L_{g2} enables the possible use of lower-cost core materials. Figure 1 also illustrates the ripple current envelopes for several key branches.

Control

Control is facilitated by the Texas Instruments (TI) TMS320F280049C microcontroller and LMG3526R030 GaN field-effect transistors (FETs). These FETs have an integrated zero-voltage-detection (ZVD) signal that is asserted anytime the switch turns on with ZVS. The microcontroller uses the ZVD information to adjust the switch timing parameters to turn the switch on with just enough current to achieve ZVS. For simplicity, Figure 2 illustrates a one-phase iTCM PFC converter. Table 1 defines the key variables used in this figure. The microcontroller uses an algorithm that solves the exact set of differential equations for the system. These equations use conditions that enforce ZVS on both switches and force the current to be equal to the current command. The equations are accurate, provided that the system is operating with the right amount of ZVS for both switches. When operating correctly, the algorithm yields the timing parameters for 0% THD and an optimal amount of ZVS. To facilitate the ZVS condition, each switch (S_1 and S_2) reports their respective ZVS turnon status on a cycle-by-cycle basis back to the microcontroller. In Figure 2, $V_{hs,zvd}$ and $V_{ls,zvd}$ denote the ZVD reporting.

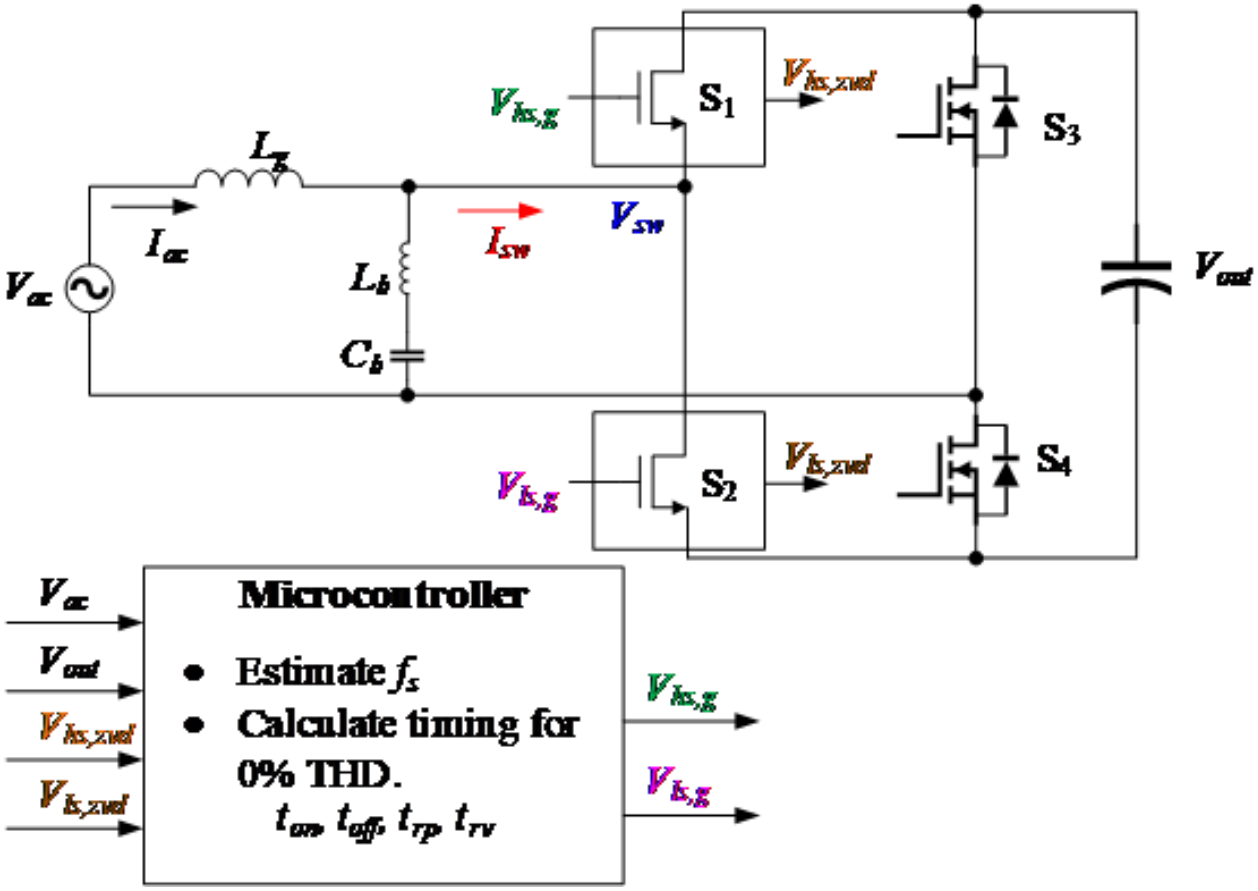

Figure 2. A single-phase iTCM schematic with control signals.

Table 1. Switch timing parameters and definitions.

Timing parameter	Definition
f_s	Switching frequency
t_{on}	This is the control switch on time; during the positive half cycle, the control switch is S_2; during the negative half cycle, the control switch is S_1
t_{off}	This is the off time of the control switch
t_{rp}	This is the dead time between the turnoff of the control switch and the turnon of the synchronous rectifier
t_{rv}	This is the dead time between the turnoff of the synchronous rectifier and the turnon of the control switch

Figure 3 illustrates the ZVD timing adjustment process. During every switching cycle, the microcontroller calculates the switch timing parameters (t_{on}, t_{off}, t_{rp}, and t_{rv}) based on the ZVD signal's cumulative history. Figure 3b shows the system operating at the ideal frequency. By ideal, I mean that the THD is 0%, and you have the perfect amount of ZVS for the high- and low-side FETs. Figure 3a shows what happens when the operating frequency is 50 kHz lower than the ideal. Notice that the high-side FET loses ZVS (as indicated by the loss of the high-side ZVD signal), while the low-side FET has more negative current than is necessary to achieve ZVS. The result is a loss of efficiency and a distorted power factor. Figure 3c occurs when the operating frequency is 50 kHz higher than the ideal. In this case, the high-side FET has ZVS but the low-side FET loses ZVS. Again, there is a clear loss of efficiency and distortion.

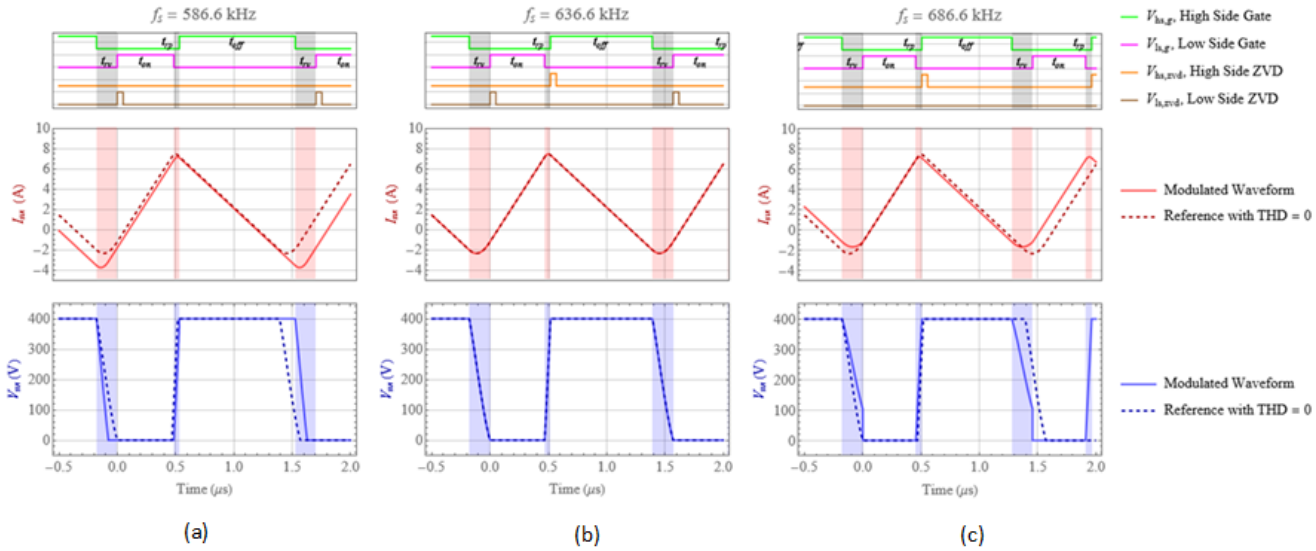

Figure 3. ZVD behavior with low f_s (a); ideal f_s (b); and high f_s (c).

Based on the presence or absence of the ZVD signal, the controller can increase or decrease the frequency to push the system to the optimum operating point. In this way, the control effort acts like an integrator that attempts to find the best operating frequency. The optimum will occur when the system is hovering right on the threshold of just barely getting ZVS every cycle.

Prototype performance

Figure 4 shows a prototype built with the topology and algorithm I've discussed so far.

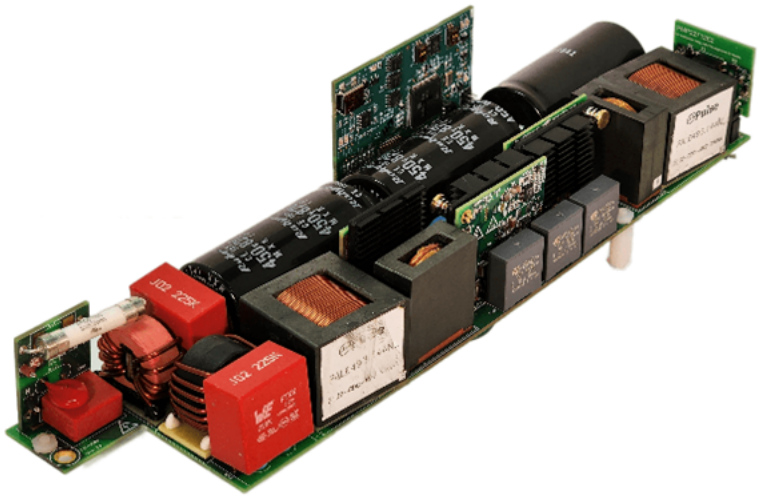

Figure 4. A 400-V, 5-kW prototype with a power density of 120 W/in^3.

Table 2 summarizes the specifications and important component values for the prototype.

Table 2. System specifications and important components

Parameters	Value
AC input	90 V-264 V
Line frequency	50-60 Hz
DC output	400 V
Maximum power	5 kW
Holdup time at full load	20 ms
L_g, low-frequency inductor	140 µH
L_b, high-frequency inductor	14 µH
C_b, high-frequency blocking capacitor	1.5 µF
THD	Open Compute Project (OCP) v3
EMI	European Standard 55022 Class A
Operating frequency	Variable, 75 kHz-1.2 MHz
Microcontroller	TMS320F280049C
High-frequency GaN FETs (S_{11}, S_{12}, S_{22}, S_{21})	LMG3526R030
Low-frequency silicon FETs (S_3, S_4)	IPT60R022S7XTMA1
Internal dimensions	38 mm × 65 mm × 263 mm
Power density	120 W/in^3

Figure 5 shows the prototype's measurement nodes and Figure 6 illustrates the system waveforms of the prototype operating under full power (5 kW). The switch-node currents, $I_{L,A}$ and $I_{L,B}$, are the sum of the current in L_g and L_b for their respective branch. The zoom section of the plot shows the waveform detail during the positive half cycle. The current waveforms have an ideal triangular shape, with just enough negative current to achieve ZVS as demonstrated by switch-node voltages V_A and V_B. Furthermore, the sinusoidal envelope of the current waveform suggests a low THD.

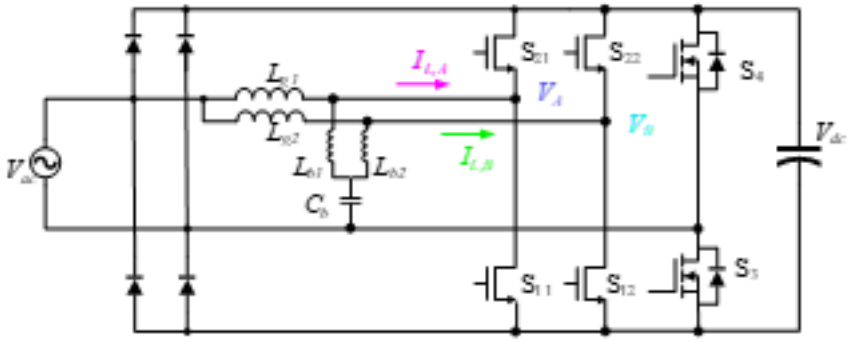

Figure 5. Prototype measurement nodes

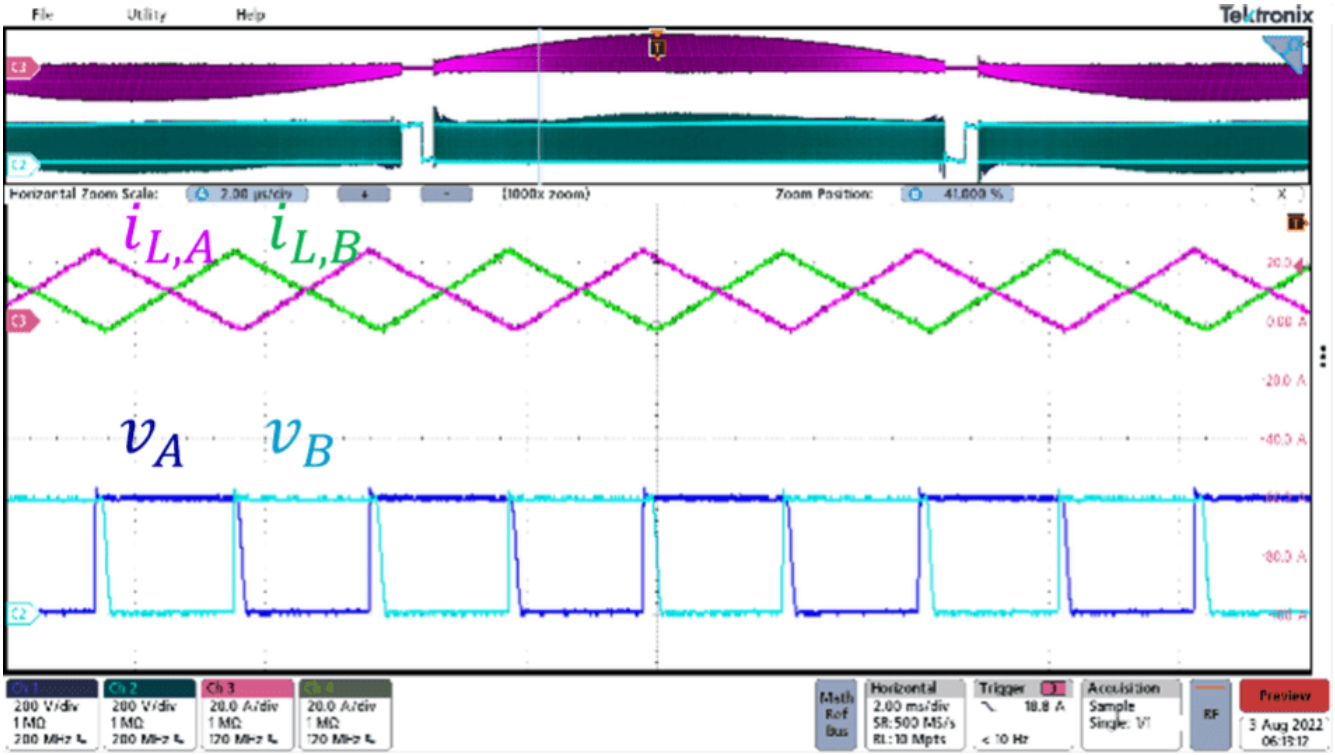

Figure 6. System waveforms of the prototype operating under full power (V_{in} = V_{out}/2, load = 5 kW, V_{in} = 230 V_{ac}, V_{out} = 400 V).

Figure 7 shows the measured efficiency and THD across the load range. The efficiency peaks above 99% and is above 98.5% for almost the entire load range. The THD has a maximum of 10% and is below 5% for most of the load range. In order to optimize performance, the unit phase sheds or adds phases at approximately 2 kW.

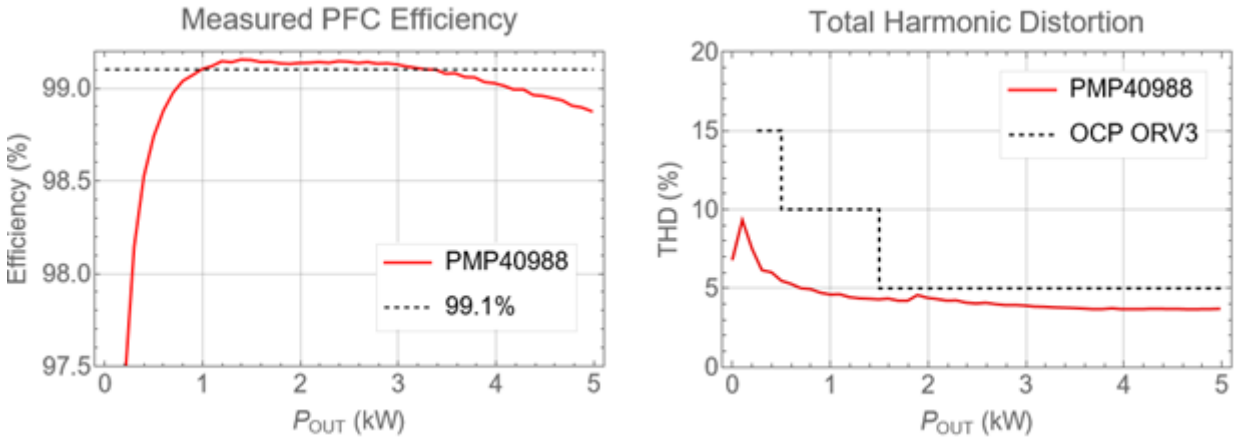

Figure 7. The prototype efficiency and THD across the load range.

Achieving a high efficiency and low THD for a totem-pole PFC

You can use the ZVD signal to control the operating frequency of a totem-pole PFC converter to achieve high efficiency and low THD. For more information about this approach, as well as a simulation model for the system, see the Variable-Frequency, ZVS, 5-kW, GaN-Based, Two-Phase Totem-Pole PFC Reference Design.

Related Content

- Power Tips #114: A potential firmware mistake may lead to control instability
- Power Tips #113: Two simple isolated power options for 8 W or less
- Power Tips #112: Onboard fixtures for fault testing
- Power Tips #111: Why current sensing is a must in collaborative, mobile robots
- PFC totem pole architecture and GaN combine for high power and efficiency
- GaN transistors for efficient power conversion: buck converters

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2. Lim, Shu Fan, and Ashwin M. Khambadkone. “A Multimode Digital Control Scheme for Boost PFC with Higher Efficiency and Power Factor at Light Load.” Published in 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Feb. 5-9, 2012, pp. 291-298. doi: 10.1109/APEC.2012.6165833.
3. Rothmund, Daniel, Dominik Bortis, Jonas Huber, Davide Biadene, and Johann W. Kolar. “10kV SiC-Based Bidirectional Soft-Switching Single-Phase AC/DC Converter Concept for Medium-Voltage Solid-State Transformers.” Published in 2017 IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), April 17-20, 2017, pp. 1-8. doi: 10.1109/PEDG.2017.7972488.
4. Liu, Zhengyang. 2017. “Characterization and Application of Wide-Band-Gap Devices for High Frequency Power Conversion.” Ph.D. dissertation, Virginia Polytechnic Institute and State University. http://hdl.handle.net/10919/77959.

Technical Article

Using interleaved ground planes to improve noise filtering from isolated power supplies

Josh Mandelcorn

Historically, automotive electronics have been powered off the same 12-V lead-acid battery used to start the vehicle. Even with surges as high as 42 V, which could occur if the generator were running and the battery cable was disconnected, voltages stay in the safety extra-low voltage (SELV) range below 60 V_{DC}. Thus, it was not necessary to worry about the spacing of conducting printed circuit board (PCB) traces to avoid electrical shock hazards in automotive circuitry.

Because electric vehicle (EV) motors need higher voltages (400 V or 800 V) to operate, shock hazards are now a concern in automotive applications. The same stringent spacings that apply to the boundary between circuitry connected to the AC mains and SELV circuits powered off of utility power now apply to the boundary between the circuitry connected to the high-voltage batteries in EVs and the SELV circuits running off the 12-V system, such as infotainment and body electronics (mainly lighting).

Failing CISPR 25

Many of the bias supplies needed to drive high-power semiconductor switches in traction inverters operating off high-voltage EV batteries are powered off the low-voltage 12-V system. The problem is that these isolated power supplies pump a lot of common-mode noise back into the 12-V car battery lines, causing them to fail the automotive Comité International Spécial des Perturbations Radioélectriques (CISPR) 25 conducted emissions limits, which extend to 108 MHz. This noise is largely driven by the main switching waveform capacitively coupling between the primary and secondary windings of the bias supply's isolation transformer. Bypass capacitors with high surge voltage ratings (Y-capacitors) between primary ground and secondary ground create a small loop to largely contain this common-mode noise, and common-mode filtering on the battery lines further reduce this noise to allow passing of CISPR 25 limits.

Spacing requirements for automotive circuitry

For reinforced spacing between high-voltage EV batteries and the low-voltage 12-V battery system used in most traditional automotive circuitry, a common target is 8 mm of spacing. This will cover 400 V_{RMS}, pollution degree 2 and material group III; or 800 V_{RMS}, same pollution degree 2, but material group I. For more details regarding spacing requirements, see the International Electrotechnical Commission (IEC) 60664-1 standard, "Insulation coordination for equipment within low-voltage supply systems Part 1: Principles, requirements and tests".

Meeting creepage and clearance requirements in multi-layer PCBs

IEC's stringent spacing requirements are driven by a high-voltage breakdown on surfaces exposed to contaminated air (creepage) and a breakdown or arcing of the air itself (clearance). Within components that bridge the primary-secondary barrier such as transformers or integrated circuits (ICs) - and likewise the inner layers of multilayer PCBs where there is no air or moisture exposure - spacing requirements are much less, as long as the barrier can withstand a several-kilovolt high-potential test. A common test level for ICs used in reinforced barrier applications is 5 kV, which allows PCBs with four or more layers to have interleaved primary and secondary grounds on the inner layers. There are spacing requirements within inner layers, but they are significantly reduced from the requirements for air-exposed layers. For some applications, a 1-mm spacing would be sufficient for 800-V battery systems.

Demo with an isolated DC/DC converter

We built two boards to demonstrate emissions performance versus CISPR 25 Class 5 limits of our UCC12051-Q1 isolated DC/DC converter. This converter was designed for 5-V input and 5-V output loaded at 100 mA with a typical battery-line electromagnetic interference filter. One board (not released) had 8-mm spacing between the primary and secondary on all four layers, and one board (the Isolated 5-V Bias Supply for Automotive CISPR 25, Class 5 Emissions, Reference Design) allowed the interleaving of primary and secondary grounds in the two inner layers, with spacing between primary and secondary grounds at 1 mm. The additional effective capacitance from primary ground to secondary ground was an estimated 11 pF. The isolated converter inside the UCC12051-Q1 switched at 8 MHz to ensure that its first frequency of CISPR 25 concern would be its fourth harmonic at 32 MHz.

Figure 1 is snippet from the isolated 5-V reference design schematic showing an IC isolated converter with capacitors from primary ground to secondary ground to contain high-frequency noise generated by the converter's isolation transformer. The unreleased board is the same as the isolated 5-V reference design, except for the lack of PCB layer interleaving.

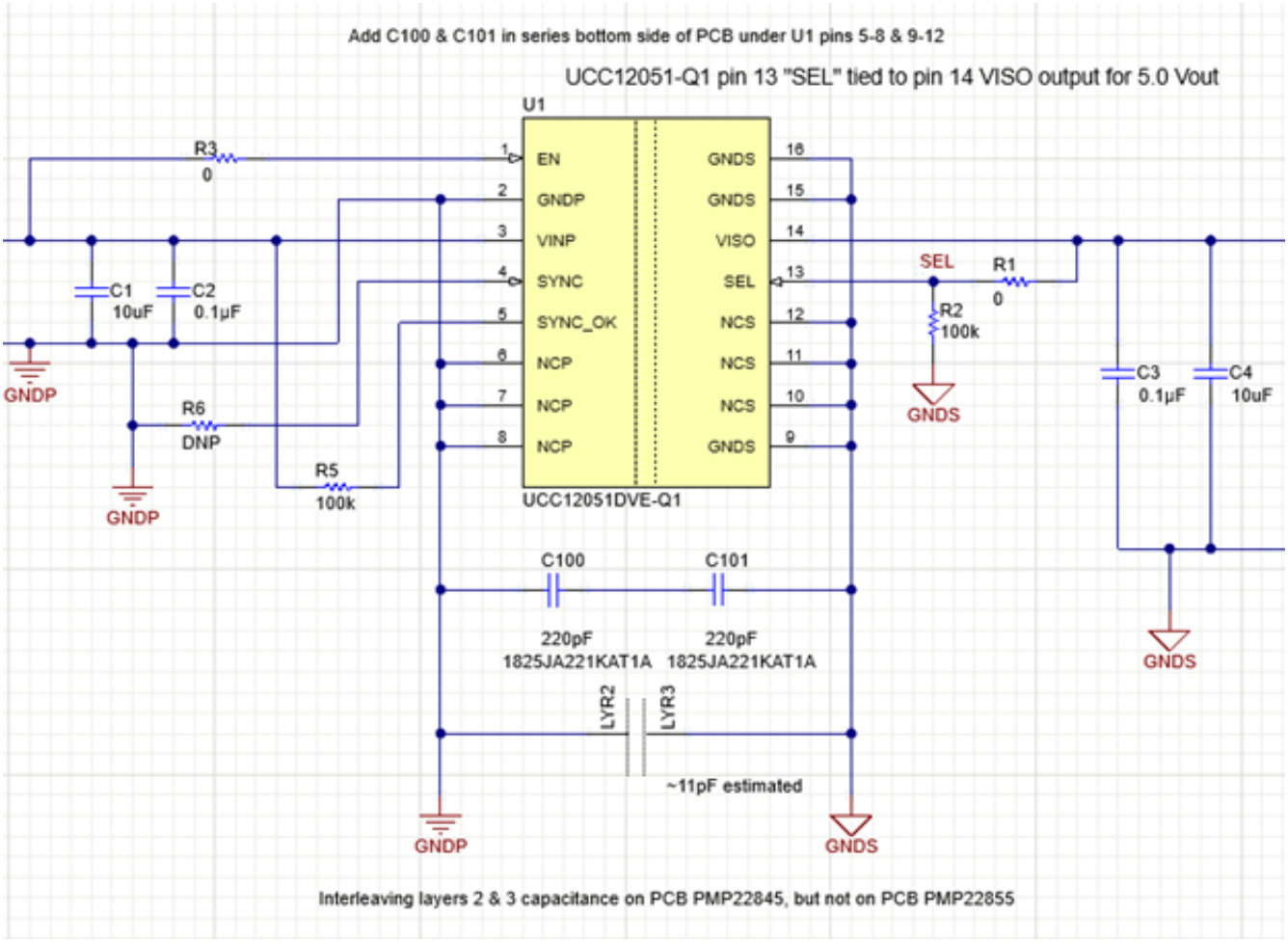

Figure 1. Primary and secondary interface of the DC/DC converter in the isolated 5-V reference design showing added bypass capacitors C100 and C101 and interleaving inner-layer capacitance. Source: Texas Instruments

Given the need for redundancy for safety and the need to maintain overall spacing from primary to secondary, we placed two Y-capacitors (C100 and C101) in series to bridge the primary and secondary grounds. Hence, the effective capacitance is one-half the value of each capacitor. Some cases will need three capacitors in series (330-pF capacitors) to maintain the necessary spacing.

In Figure 2, the image on the left is the not released board with 8-mm spacing for all layers; the image on the right is the isolated 5-V reference design with the top and bottom layers having 8-mm spacing and the inner layers having only 1-mm spacing, allowing them to have overlapping primary and secondary ground planes.

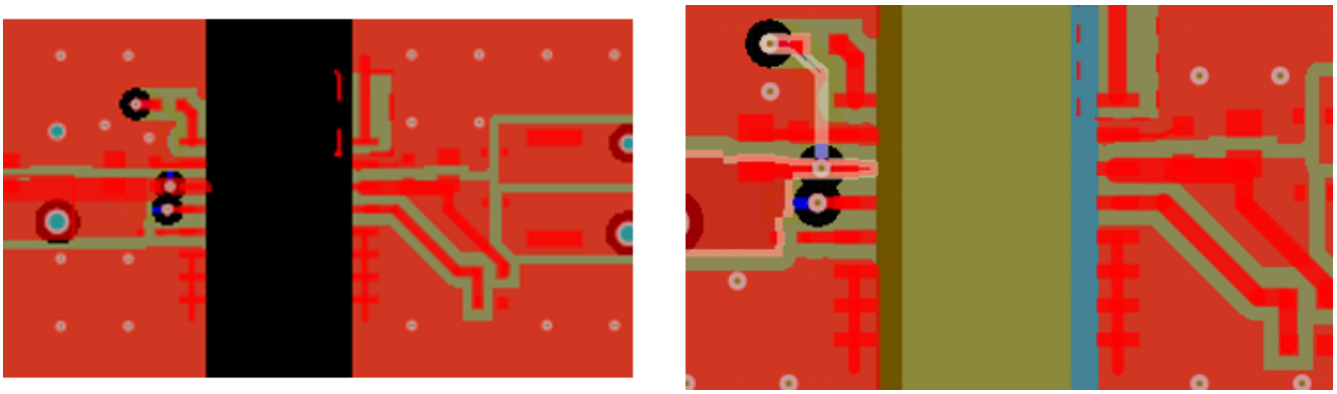

Figure 2. 8-mm spacing on all layers (left) versus 8-mm spacing on only the top and bottom layers (right): top layer is red; layer 2 is dark green; layer 3 is light blue; layer 4 is tan; overlap of layers 2 and 3 are light green; no copper on any layer is black. Source: Texas Instruments

Radiated emissions versus CISPR 25

With the isolated 5-V reference design, we expected that this interleaving, with its added 11 pF of capacitance between primary and secondary grounds, would only help radiated emissions above 200 MHz. And indeed, the interleaving layers allowed radiated emissions to pass CISPR 25 Class 5 for all frequencies above 200 MHz, even without bypass capacitors C100 and C101 (Figure 3). Without the interleaving layers, we needed additional Y-capacitors between primary and secondary grounds to pass in the same frequency range. See the test report for the emissions test setups.

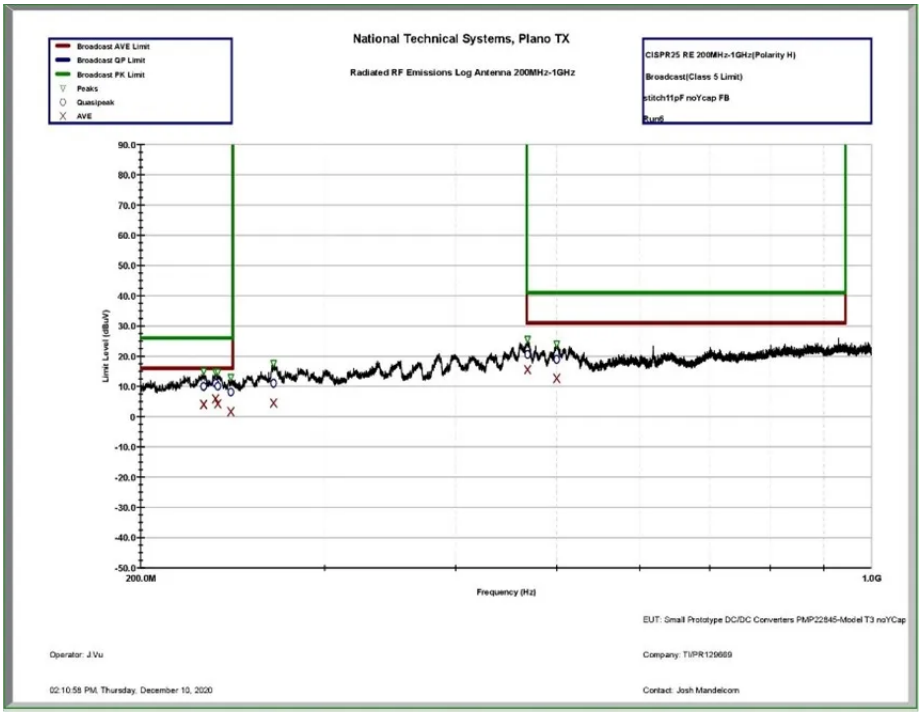

Figure 3. Radiated emissions versus CISPR 25 Class 5 above 200 MHz without any additional Y capacitors. This specific scan is not in the isolated 5-V reference design test report. The board passed limits with greater than 10 dB of margin. Source: Texas Instruments

The surprise was that filtering (C101 and C102) for the 30- to 108-MHz range, with its stringent conducted emissions limits, was significantly enhanced. With 110 pF of effective additional capacitance between primary ground and secondary ground, the interleaving improved the conducted noise reduction throughout the entire 30- to 108-MHz range by about 4 to 8 dB. Over this frequency range, the interleaving converted a failure by 4 dB to a pass with 4 dB of margin.

Conducted emissions versus CISPR 25

Figure 4 and Figure 5 show the conducted emissions scans of these two boards, with the only difference being the inner-layer interleaving. Both scans were on the same line impedance stabilization network (LISN), with the same common-mode battery line filtering and the same loading of 100 mA off the 5-V output.

Figure 4. Isolated 5-V reference design (with interleaving layers) conducted emissions versus CISPR 25 Class 5, 30 to 108 MHz: passed with 4.5 dB of margin, with the worst case being a "CISPR average" detection at 82 MHz. Source: Texas Instruments

Figure 5. Unreleased board (no interleaving layers) conducted emissions versus CISPR 25 Class 5, 30 to 108 MHz: failed by 3.8 dB of margin, with the worst case being a CISPR average detection at 32 MHz. Source: Texas Instruments

The interleaving layers with the estimated 11 pF of capacitance contributed far more to the filtering than adding 11 pF to the effective 110 pF of capacitance of the Y-capacitors, which would improve filtering by about 1 dB. The inner-layer ground planes reduce the effective inductance of the bridging Y-capacitors and allow them to better shunt these high-frequency harmonics.

This filtering improvement adds to the benefits of close-in ground planes, improving the performance of capacitor filtering whether the goal is to limit output noise, control emissions in non-isolated applications, or reduce stresses and failures on semiconductors.

Related Content

- Power Tips #117: Measure your LLC resonant tank before testing at full operating conditions
- Power tips #116: How to reduce THD of a PFC
- Power Tips #115: How GaN switch integration enables low THD and high efficiency in PFC
- Stop EMI from spreading in an EV design
- A new EMI threat?

Additional resources

- Use the PCB creepage calculator for reinforced isolation double results.
- Check out more from Texas Instruments:
  - "How to Meet the Higher Isolation Creepage & Clearance Needs in Automotive Applications."
  - "Power Tips: The Ground Plane – A Critical Element in Noise Management of Switching Regulators."
  - "Power-Conversion Techniques for Complying with Automotive Emissions Requirements."
  - "Reduce Buck-Converter EMI and Voltage Stress by Minimizing Inductive Parasitics."

Relevant standards

- IEC 60664-1 Insulation Coordination for Equipment Within Low-Voltage Supply Systems – Part 1: Principles, Requirements and Tests
- IEC 61800-5-1 Adjustable Speed Electrical Power Drive Systems – Part 5-1: Safety Requirements – Electrical, Thermal and Energy
- Institute for Interconnecting and Packaging Electronic Circuits (IPC) 2221B Generic Standard on Printed Board Design
- CISPR 25 Ed. 5.0 b 2021 Vehicles, Boats and Internal Combustion Engines – Radio Disturbance Characteristics – Limits and Methods of Measurement for the Protection of On-Board Receivers

Technical Article

Snubbing the flyback converter

Robert Kollman

In October, we described how to snub the voltage across output rectifiers at turn on in the forward converter. Now, we look at snubbing the FET turn off voltage in the flyback converter.

Figure 1 shows the flyback converter power stage and the primary MOSFET voltage waveform. This converter operates by storing energy in the primary inductance of a transformer and releasing the energy into the secondary when the MOSFET is turned off.

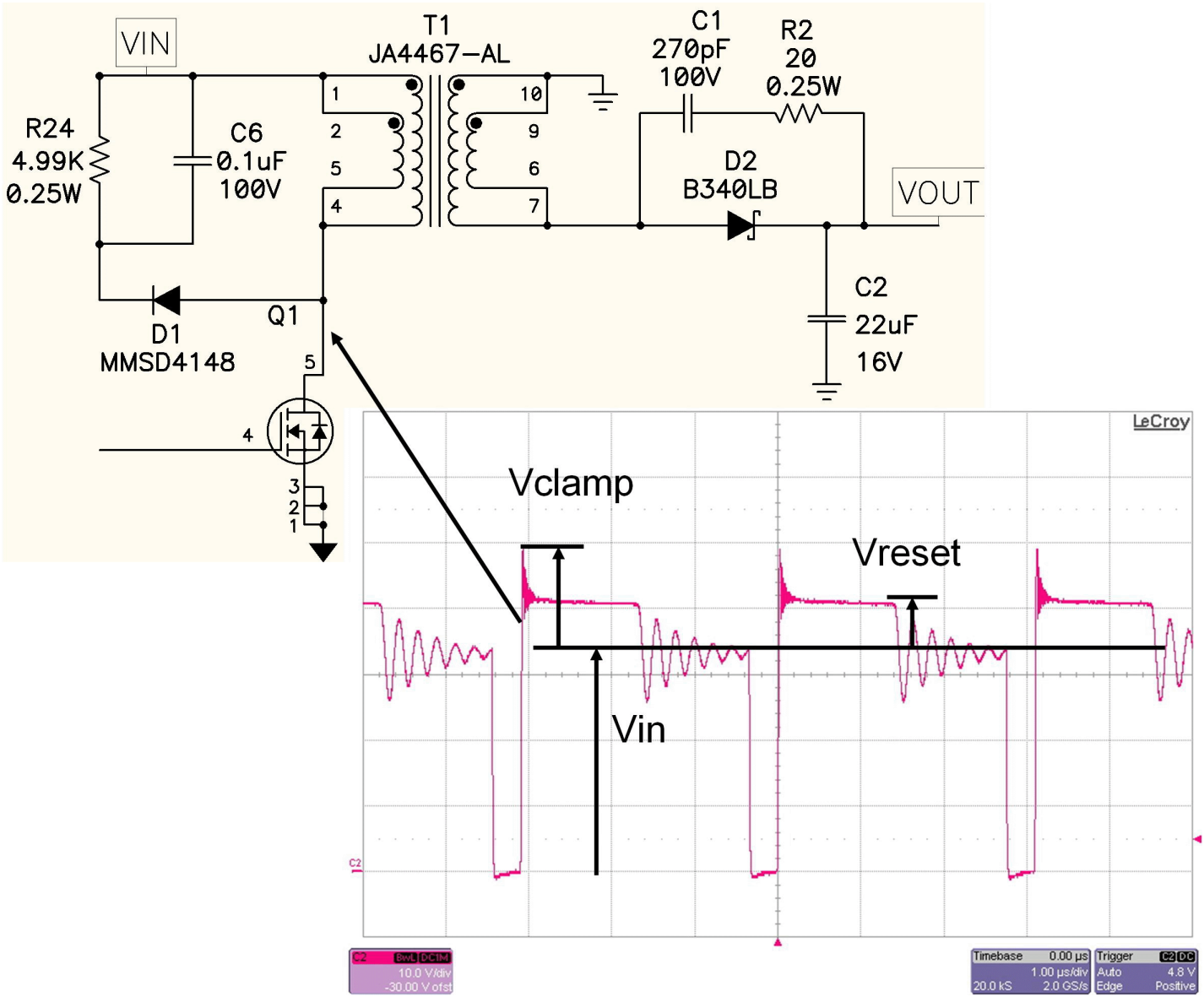

Figure 1. Leakage inductance creates excessive voltage at FET turn off.

A snubber is often needed when the MOSFET is turned off as the transformer's leakage inductance will cause the drain voltage to rise above the reflected output voltage (V_{reset}). The energy stored in the leakage inductance can avalanche the MOSFET, so a voltage clamping circuit comprising of D1, R24 and C6 is added. The clamp voltage on this circuit is set by the amount of energy in the leakage and the power dissipation in the resistor. A lower-value resistor will lower the clamp voltage, but will increase the power loss.

Figure 2 shows the transformer primary and secondary current waveforms.

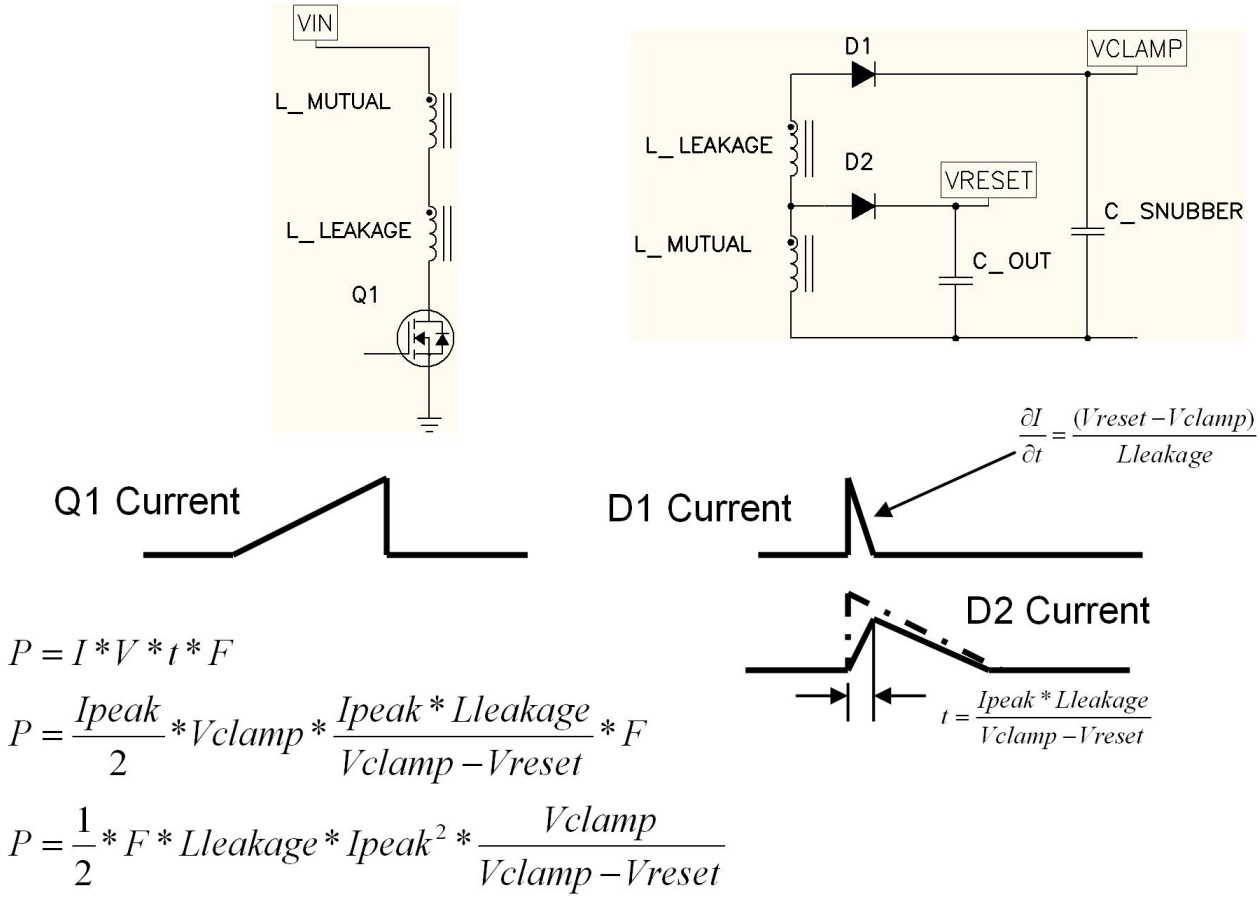

Figure 2. Leakage inductance steals the output energy.

On the left is the simplified power stage when the MOSFET is on. The input current ramps up through the series combination of leakage and mutual inductance. The right shows a simplified circuit during the off period. Here the voltage has reversed to the point that the output diode and clamp diode are forward biased. We show the output capacitor and diode reflected to the primary side of the transformer.

The two inductors are in series and are initially carrying the same current when Q1 turns off. That means that there is no current flow in the output diode D2 immediately after turn off and the total transformer current flows in D1. The voltage across the leakage inductance is the difference between the clamp and reset voltage and will tend to discharge the leakage rapidly.

As shown, it is a simple calculation to determine the energy diverted to the snubber. It turns out that you can reduce the diverted energy by reducing the time it takes to discharge the energy in the leakage inductance. This is accomplished by allowing the clamp voltage to increase.

Interestingly, you can calculate the trade-off between clamp voltage and snubber power dissipation. As shown in Figure 2, the power put into the clamp circuit is equal to the average clamp diode current times the clamp voltage (assuming a constant clamp voltage). Rearranging some terms we find the term ½ × F × L × I^2, which relates to the output power of a discontinuous flyback converter. In this case, the inductance is the leakage inductance.

The expression is a little surprising in that the power loss is not just the energy stored in the leakage. It is always greater, but with a dependency on the clamp voltage. Figure 3 shows this relationship.

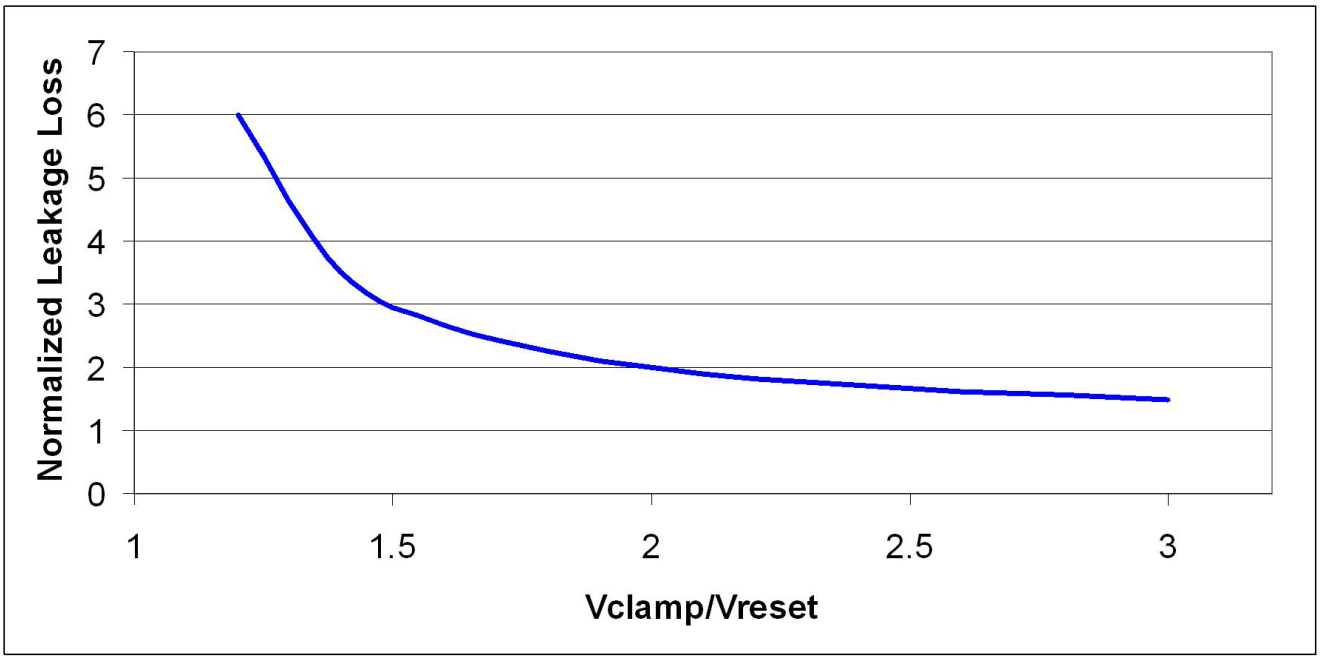

Figure 3. Increasing the clamp voltage reduces snubber loss.

The graph plots the loss normalized to the leakage inductance energy loss versus the ratio of the clamp to reset voltage. At high values of clamp voltage, the snubber loss approaches the energy in the leakage inductance. As the clamp voltage is reduced by reducing the resistance, energy is diverted from the main output and the snubber dissipation increases dramatically. At a Vclamp/Vreset ratio of 1.5, it is almost three times the loss associated with the leakage inductance stored energy.

Coincidentally, the leakage inductance is often on the order of 1% of the magnetizing inductance. This makes Figure 3 even more interesting, in that it gives us an indication of the impact on efficiency that lowering the clamp voltage will have. The vertical axis then just becomes efficiency loss. So reducing the clamp ratio from 2 to 1.5 will have a one percent efficiency impact.

To summarize, the leakage inductance of a flyback converter can put an unacceptable voltage stress on the power switch. An RCD snubber can control the stress. However, there is a trade-off between the clamp voltage and circuit losses.

Technical Article

Isolating a SEPIC

John Betten

If someone asked you what topology to use for an isolated, low-power output, chances are your first thought would be a flyback. Although a flyback is an excellent topology with benefits such as low cost, low component count and ease of adding additional outputs, it still has several drawbacks. The field-effect transistor (FET) and rectifier ringing associated with flyback transformer leakage inductance create electromagnetic interference (EMI), raise component stresses and lower efficiency. Additionally, obtaining well-regulated voltages can be a challenge when there are multiple outputs, especially with wide load variations. Let's see how isolating a single-ended primary-inductor converter (SEPIC) can provide an alternate approach and alleviate some of these issues.

The SEPIC is a nonisolated topology. However, as with a flyback, you can easily add additional transformer windings to create isolated outputs. The simplified schematic of Figure 1 shows a standard SEPIC converter generating a single nonisolated output on the left, with two additional isolated outputs on the right. The first isolated winding supplies a nominal 6V output as an input to a 5V linear regulator. The second isolated winding is stacked on top of the first to create a nonregulated 12V output.

You want tight coupling between the transformer winding of V_{OUT1} and the isolated windings (V_{OUT2}, V_{OUT3}), since energy in these windings simultaneously transfers to all three outputs. Leakage inductance between these windings only serves to degrade their voltage regulation. However, tight coupling is **not** required between the SEPIC's primary winding and the V_{OUT1} winding. Minimal FET ringing exists because capacitor C_{AC} provides a low impedance path for leakage energy into V_{OUT1} when the boost FET turns off. Since the SEPIC's primary winding voltage waveform has considerably less ringing than a flyback, this leads to improved output voltage regulation, especially under extreme crossload conditions where spike peak-detection often occurs.

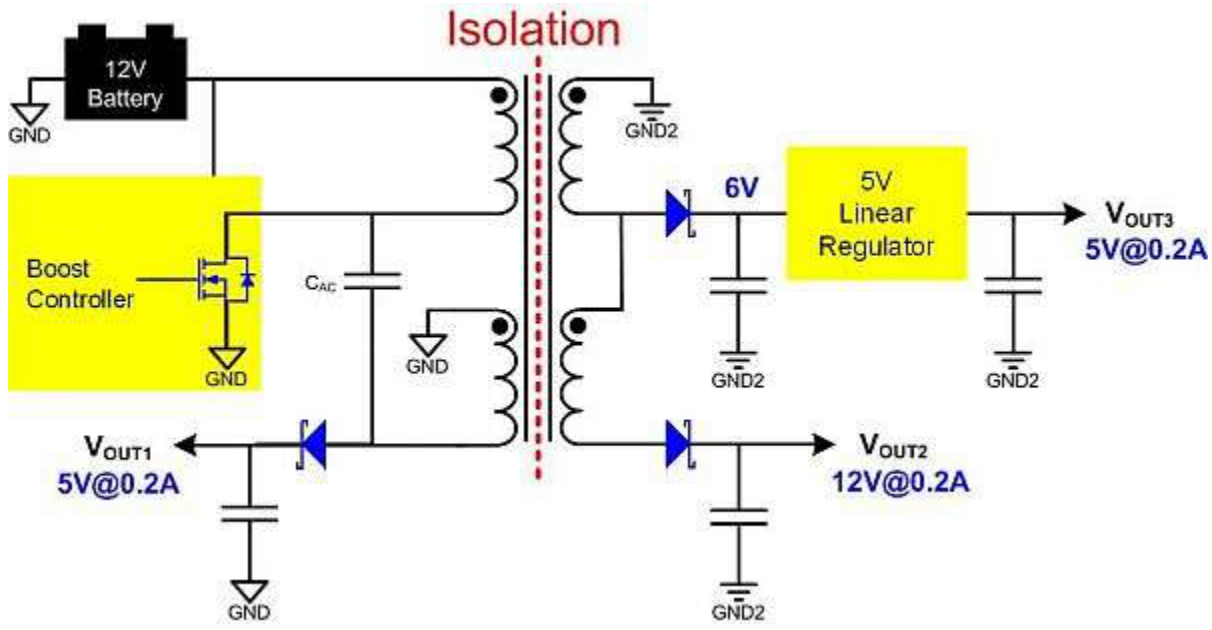

Figure 1. A SEPIC converter with additional windings provides isolated outputs.

As in all SEPICs, the turns ratio between the primary and V_{OUT1} must be 1-to-1. All other outputs are not bound to this turns ratio, however, and you can adjust them to provide any required output voltage, which you can easily calculate with Equation 1:

$$\frac{N_x}{N_1} = \frac{V_{OUT\,x} + V_{diode\,x}}{V_{OUT\,1} + V_{diode\,1}} \quad (1)$$

Figure 2 shows the difference in FET voltage ringing between a SEPIC and a flyback. You can obtain the flyback FET voltage waveform from the SEPIC circuit simply by removing C_{AC}, which converts it into a flyback. The elimination of ringing on the FET significantly reduces the uncoupled energy conducted into the isolated outputs, improving regulation.

Figure 2. The voltage on a SEPIC FET rings less than a flyback, lowering stress and improving output voltage regulation.

Figure 3 shows the test circuit schematic used to obtain the regulation data in Figure 4, while Figure 5 shows a photo of the actual hardware. This design uses primary-side feedback for a regulated voltage on V_{OUT1}. The isolated outputs rely on a combination of tight transformer coupling and small pre-loads to obtain reasonable voltage regulation. Since the linear regulator holds the isolated 5V output constant, its minimum and maximum inputs are of primary concern. If the input to the linear regulator is too low, the output voltage can drop out. Conversely, if the input to the linear regulator is too high, excess power will dissipate.

Regulation data for the isolated outputs show that their worst-case minimum and maximum voltages occur during extreme crossload conditions. You can see minimum voltages on the isolated windings while they are at maximum loads with V_{OUT1} unloaded. Maximum voltages on the isolated windings occur at no load with V_{OUT1} at maximum load. Based on the test data, I measured a variation in regulation of less than ±4%. Although these results are not indicative of all designs, they suggest that similar designs can reasonably achieve ±5% voltage regulation, while flybacks are more likely to be at least several percent higher.

It's possible to greatly improve the cross-regulation of flybacks by implementing synchronous rectifiers, as Brian King described in Power Tips #78. However, this improvement requires the use of higher-cost FETs and additional drive circuitry. You can apply this same technique to isolated SEPIC converters, but the rectifier for the nonisolated output would also need to be synchronous. I described how to easily implement a synchronous SEPIC in a previous TI blog post.

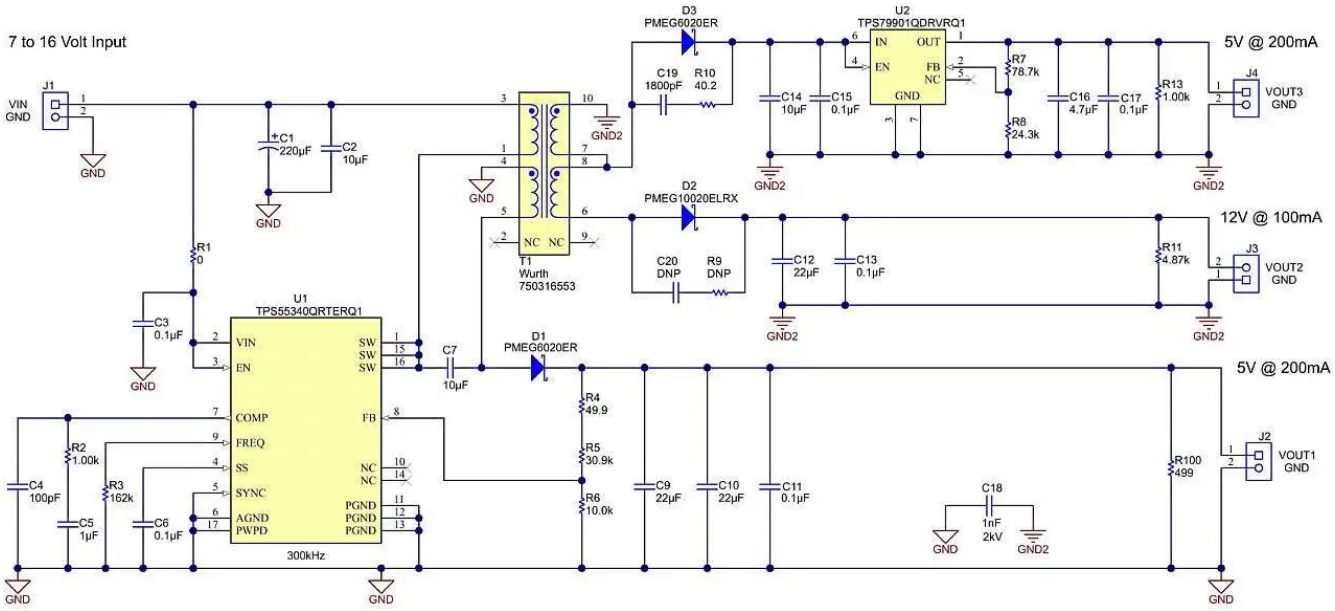

Figure 3. Actual SEPIC design with dual isolated outputs.

Voltage Regulation Data							
VIN (V)	VOUT 5V #1 (V)	IOUT 5V #1 (mA)	LDO In (V)	LDO out (V)	IOUT LDO (mA)	VOUT 12V (V)	IOUT 12V (mA)
No Load Conditions							
7	5.04	0	6.07	5.06	0	11.88	0
12	5.04	0	6.08	5.06	0	11.88	0
16	5.04	0	6.08	5.06	0	11.89	0
Full Load Conditions							
7	5.04	200	5.96	5.06	200	11.78	100
12	5.04	200	6.02	5.06	200	11.85	100
16	5.04	200	6.03	5.06	200	11.86	100
Cross Loading							
7	5.04	0	5.77	5.06	200	11.39	100
7	5.04	200	6.23	5.06	0	12.14	0
12	5.04	0	5.82	5.06	200	11.46	100
12	5.04	200	6.24	5.06	0	12.13	0
16	5.04	0	5.86	5.06	200	11.54	100
16	5.04	200	6.24	5.06	0	12.12	0
			6.005	High/Low Avg (V)		11.765	High/Low Avg (V)
			-3.91	Percent Low (%)		-3.19	Percent Low (%)
			3.91	Percent High (%)		3.19	Percent High (%)

Figure 4. Measured voltage regulation data.

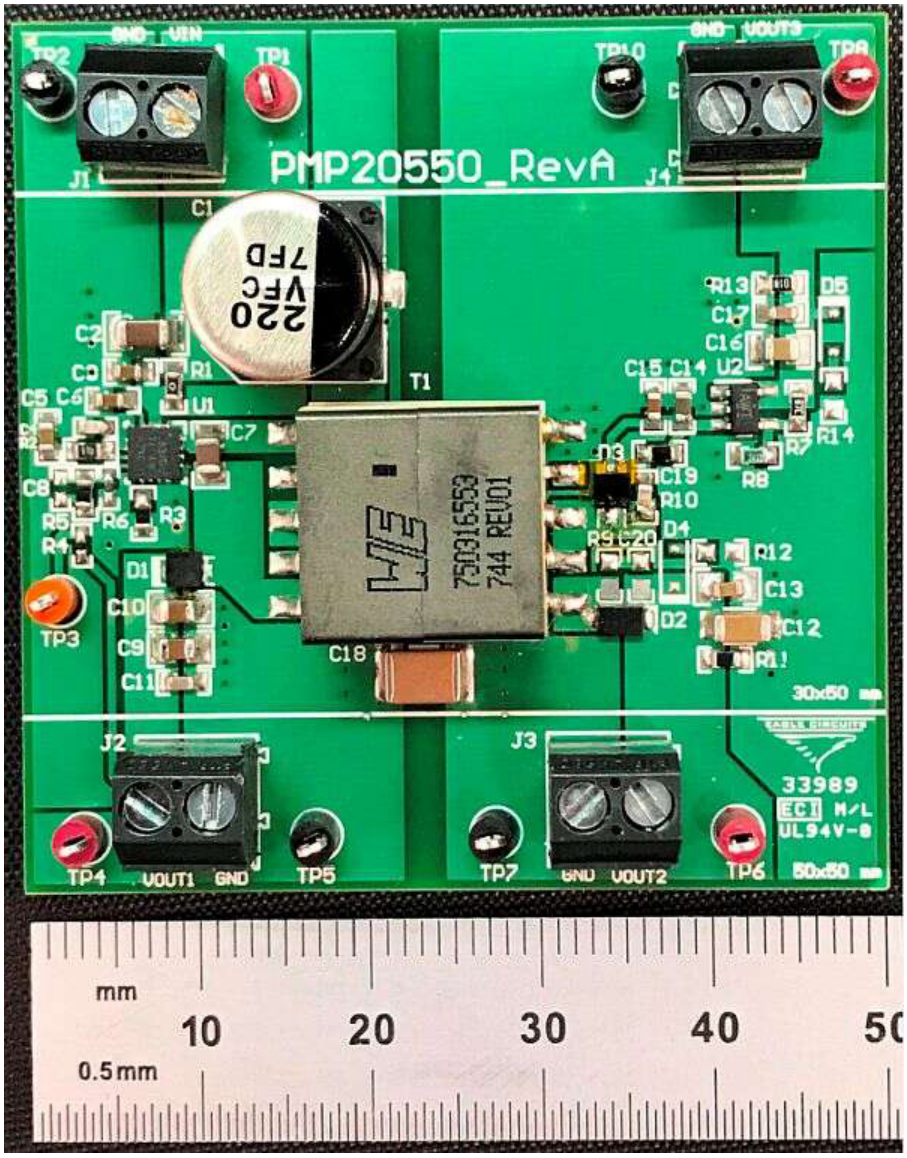

Figure 5. Prototype circuit hardware.

An isolated SEPIC converter may not be your first choice for adding an isolated output voltage, but it offers higher immunity to leakage inductance associated ringing than a flyback, which can improve output voltage regulation. This may eliminate the need for additional post regulation, resulting in cost savings.

See more of TI's Power Tips on Power House.

Related articles

- Guess what: underutilized SEPIC outperforms the flyback topology
- SEPIC/Ćuk converter sprouts second output

Previously published on EDM.com.

Technical Article

Compensating for diode drop variations

John Betten

As useful as the rectification properties of diodes are, the forward voltage drop they create can vary widely with temperature. This increases losses and can introduce tolerance errors in power supplies.

While it may not be possible to eliminate their losses, it is possible to use diodes in ways that can reduce tolerance errors in certain applications. This article will provide three examples that will show you how to achieve this.

You can build a simple low-current voltage regulator from a resistor and a Zener diode. This type of regulator is often adequate for noncritical applications such as internal bias voltages. The circuit generally regulates the output voltage to about ±10% tolerance. However, it may be possible to improve the regulation by adding a diode in series.

Figure 1 shows the addition of a diode in series with the Zener diode. The curve in Figure 1 plots the temperature coefficient for various Zener voltages. Above values of 4.7V, the temperature coefficient becomes increasingly positive, so as the operating temperature increases, the voltage across the Zener diode increases. If paired with the negative temperature coefficient of a diode, the increase of the Zener voltage will be offset in part by the decrease in the diode forward voltage, resulting in temperature error cancellation.

Zener values below 4.7V have a negative temperature coefficient, so adding a diode in series would actually increase regulation errors.

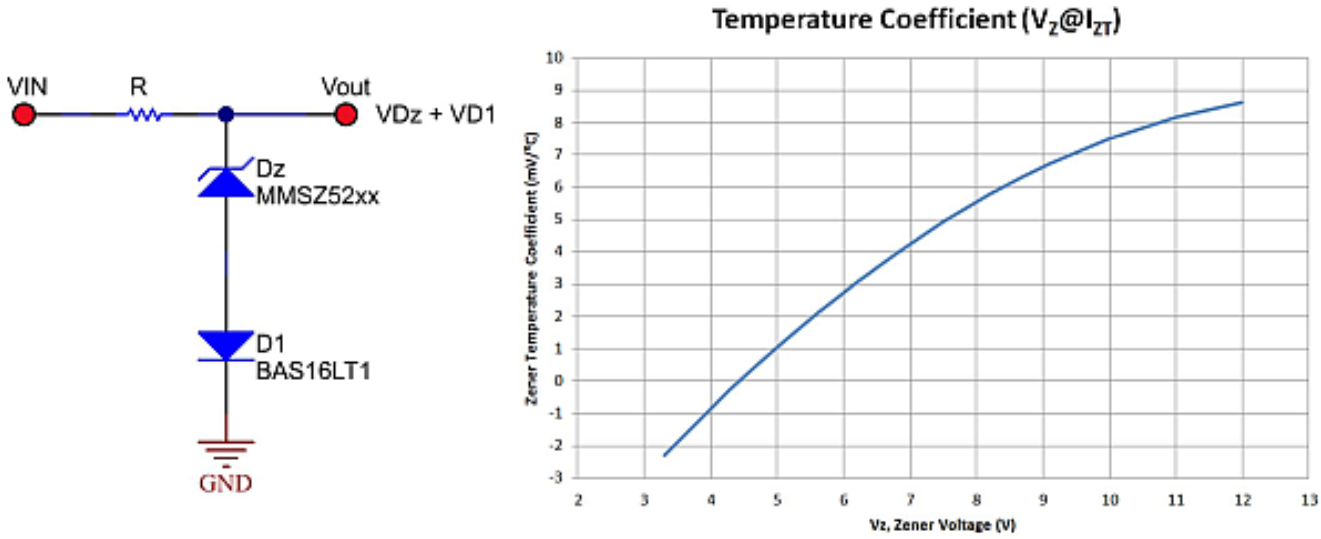

Figure 1. A positive-temperature coefficient Zener diode in series with a negative-temperature coefficient diode can reduce temperature errors.

As an example, a 7.5V Zener diode shows a temperature coefficient of +5mV/° C, while a conventional diode (BAT16) is about −1.6mV/° C at 10mA. This value becomes increasingly more negative (−3mV/° C) with very small diode currents, so be sure to check it at the current level of the Zener diode. Ideally, the two temperature coefficients would perfectly cancel out, but that is not realistic or always necessary, as a simple improvement may be sufficient. For higher-voltage Zener diodes with even higher positive-temperature coefficients, two (or more) diodes could improve cancellation.

Figure 2 shows the calculated voltage regulation error of Figure 1 versus the output voltage for various Zener values – without series diodes, with one series diode and with two series diodes – operating between 25° C and 100° C. The vertical line in Figure 2 shows that adding series diodes can reduce temperature-dependent errors by 3-5% for a 7.5V output.

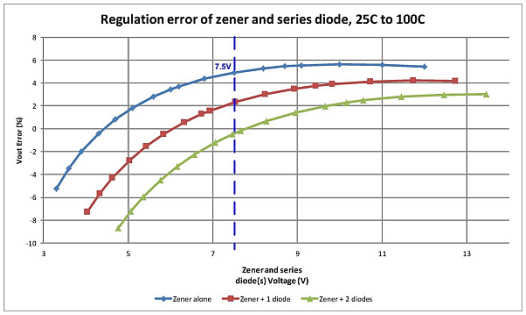

Figure 2. Adding one or more diodes in series with a Zener value over 4.7V reduces voltage regulation errors.

The second example involves converters that require a level shifter to send the output voltage information to the control circuit.

Figure 3 is a negative-input to positive-output inverting buck-boost. The control circuit is referenced to the −Vin rail, but the output voltage is referenced to GND. For the control circuit to accurately regulate the output voltage, the level shifter recreates the differential “Vout to GND” voltage between “FB and −Vin.” In this implementation, a current source approximately equal to (V_{out} − $V_{be\ Q1}$)/R flows from Vout to −Vin. This current flows in the lower resistor to reconstruct the output voltage referenced to −Vin. Adding Q2, configured as a diode, restores the Vbe drop lost from Q1. The level-shifted voltage at the FB pin now closely replicates that between Vout and GND, except for a small error related to beta.

One benefit of adding “diode” Q2 is that its forward voltage will be quite close to that of Q1, since almost the exact same current flows through both. To achieve the best voltage matching on Q2, you should use the same transistor as Q1. Another benefit is that both transistors have the same temperature coefficients, allowing their forward voltages to track each other more precisely. The temperature error associated with Vbe variations are significantly reduced since they cancel each other out (V_{FB} ~ V_{out} −$V_{be\ Q1}$ + $V_{be\ Q2}$). It’s important to locate the Q1 and Q2 near each other so that they are exposed to the same temperature, or if possible, to use a dual-transistor package.

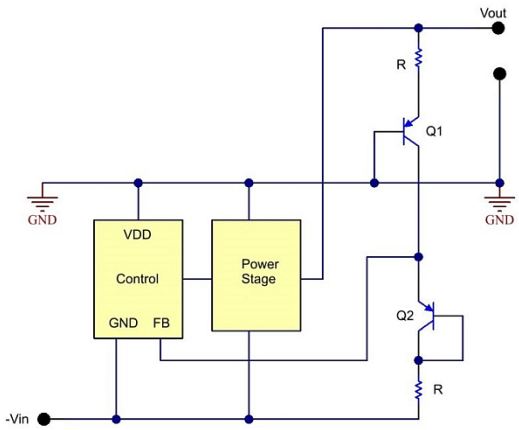

Figure 3. A level shifter implements Q2 to cancel variations related to Q1.

The third example shown in Figure 4 shows a boost converter with a series of charge-pump stages, where each stage “n” adds approximately “V1” to the total output at “Vn + 1.” For more details on voltage multiplier operation, see “Power Tips: Multiply your output voltage.”

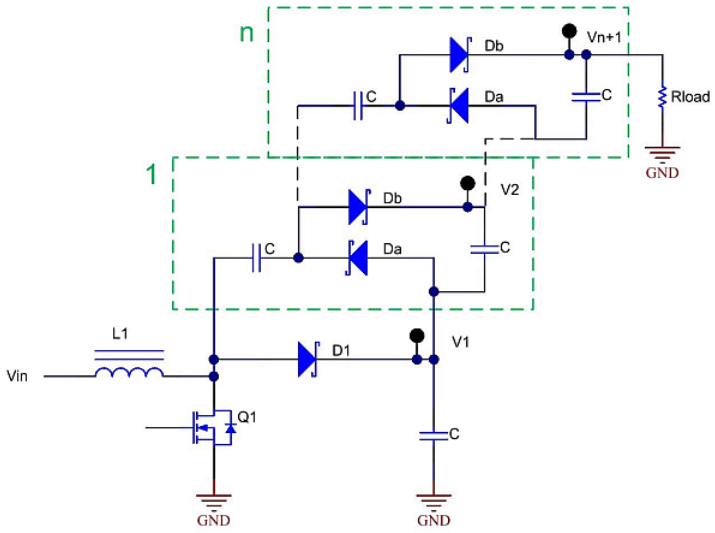

Figure 4. Charge-pump diode drops can offset each other.

Equation 1 approximates the total output voltage as:

$$V_{n+1} \sim \left(n+1\right) \times V1 + n\left(V_{D1} - V_{Da} - V_{Db} - \frac{I\,load}{fsw \times C}\right),\ n = charge\ pump\ stages \quad (1)$$

From Equation 1, you can see that V_{n+1} is largely determined by multiples of *n*, but reduced by the "error terms" related to diode forward drops and the charge-pump transfer capacitor's ripple voltage. Assuming that all diodes are the same type and that their forward voltages are equal:

$V_{D1} = V_{Da} = V_{Db}$, then Equation 2 is:

$$V_{n+1} \sim \left(n+1\right) \times V1 - n\left(V_{D1} + \frac{I\,load}{fsw \times C}\right) \quad (2)$$

In Equation 2, the "error terms" on the right side reduce the output below its ideal *n* + 1 multiple. To improve this, using Schottky diodes for V_{Da} and V_{Db} and a conventional diode for V_{D1}, with forward voltage drops equal:

$V_{Da} = V_{Db} = V_{D1}/2$, then Equation 3 is:

$$V_{n+1} \sim \left(n+1\right) \times V1 - n\left(\frac{I\,load}{fsw \times C}\right) \quad (3)$$

From Equation 3, you can see that it is possible to reduce the error terms associated with the diode drops, thereby increasing the output voltage further. While Equation 3 is still an approximation, the concept is valid in that the output voltage will increase.

Diode forward voltage and temperature variations often degrade circuit performance, but that doesn't always have to be the case. These design examples demonstrate methods in which it's possible to cancel or minimize the temperature-dependent characteristics of diodes.

Check out TI's Power Tips blog series on Power House.

Also see :

- Easily measure diode capacitance and reverse recovery
- Power Tips #79: Load transient testing with high slew rates

Technical Article

A potential firmware mistake may lead to control instability

Desheng Guo and Aki Li

When designing a digital power supply such as boost power factor correction (PFC), have you ever seen a current oscillate like it does in Figure 1?

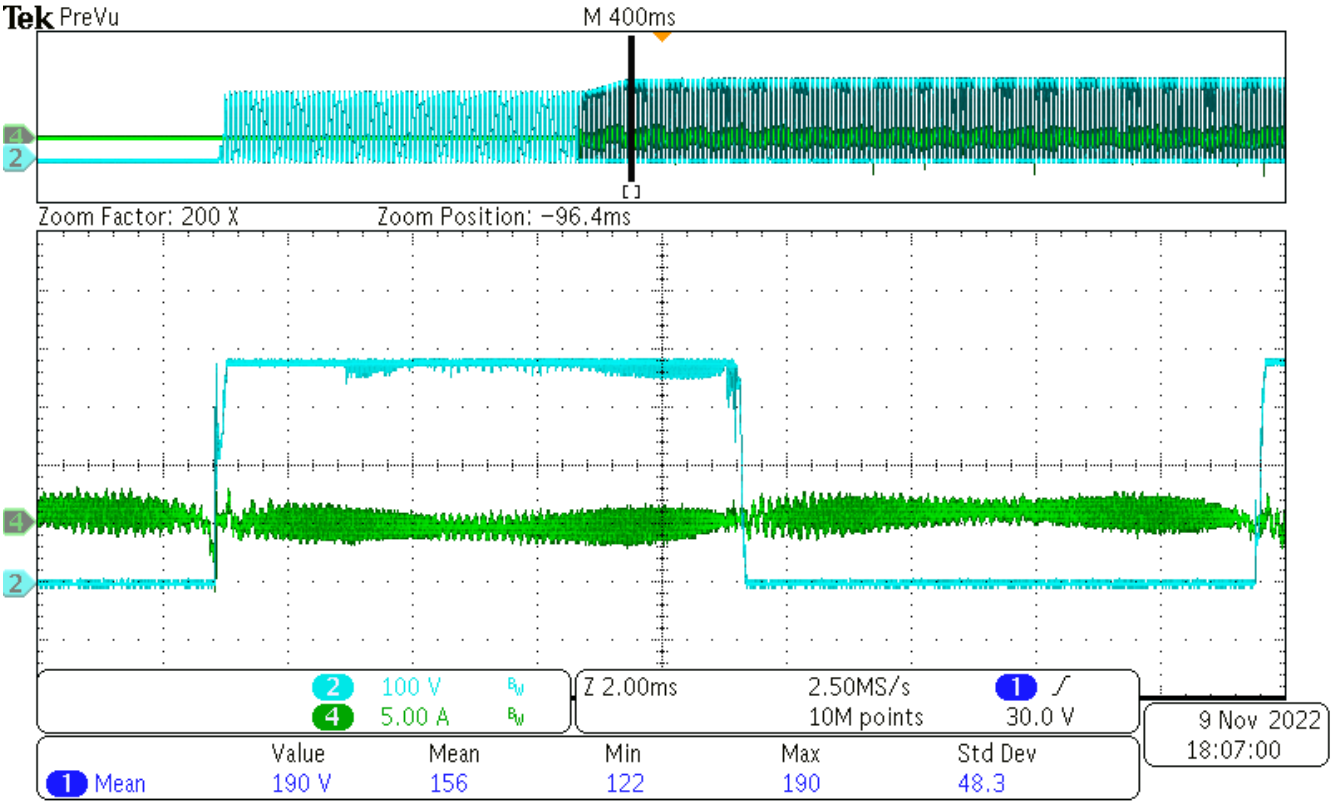

Figure 1. Current oscillation happens in the PFC stage. Source: Texas Instruments

You may think that this unstable oscillation is caused by a too-fast control band, so you reduce the proportional gain (Kp) and integral gain (Ki) of the proportional-integral (PI) controller and significantly reduce the cross frequency. Then the oscillation disappears.

But is that the best solution? The lower current-loop bandwidth reduces the control speed, but you may find that the total harmonic distortion (THD) test fails. And sometimes the oscillation appears again when your source impedance is a little bit large.

Is there another possible cause of this instability? How can you achieve the best control bandwidth with enough phase margin? Let's analyze the digital control loop in detail, to see how this potential mistake was introduced. We will also show you how to check whether this instability is happening in your control firmware.

MCU-based digital control

Figure 2 illustrates an MCU-based digital control system.

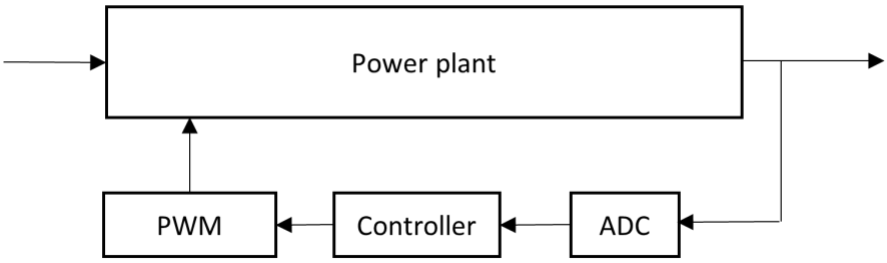

Figure 2. The digital control system is built around a microcontroller. Source: Texas Instruments

The control loop includes an analog-to-digital converter (ADC) for sampling the object current/voltage, a digital controller for generating the adjust value, and a pulse-width modulator (PWM) for executing the adjustment, changing the target current/voltage by changing the duty or frequency.

ADC sampling in a switched-mode power supply (SMPS) is often at the middle points of two switching cycles, which not only avoids noise disturbances from switching, but also gets the average current value of the power inductor in continuous conduction mode (CCM).

The digital controller is calculated in an interrupt service routine (ISR) and could be triggered synchronously with the PWM output. The trigger event could be one of these occurrences: the PWM's "COUNTER" equals "ZERO," "PERIOD," or a specific value "CMP."

It is not possible to update the PWM immediately when the controller completes all calculations, but the PWM registers must be loaded by shadow registers at a dedicated moment, such as when the PWM counter equals "ZERO" or "PERIOD". If the PWM values are changed while the counter is rising or falling, it is very possible to generate false PWM action, missing pulses or duplicating pulses.

Unlike an analog control system, digital control is executed by the sampling frequency, and there must be a delay time (T_d) from sampling to reloading a new value to the PWM. PWM modification is implemented by adjusting the flipping moments, which happens once with single-edge modulation (count up/count down mode), and happens twice with dual-edge modulation (count up-down mode). So, the minimum T_d will be one switching cycle T_s, (as shown in Figure 3a) or one-half switching cycle $T_s/2$, (as shown in Figure 3b), depending on the modulation reloading frequency that you choose.

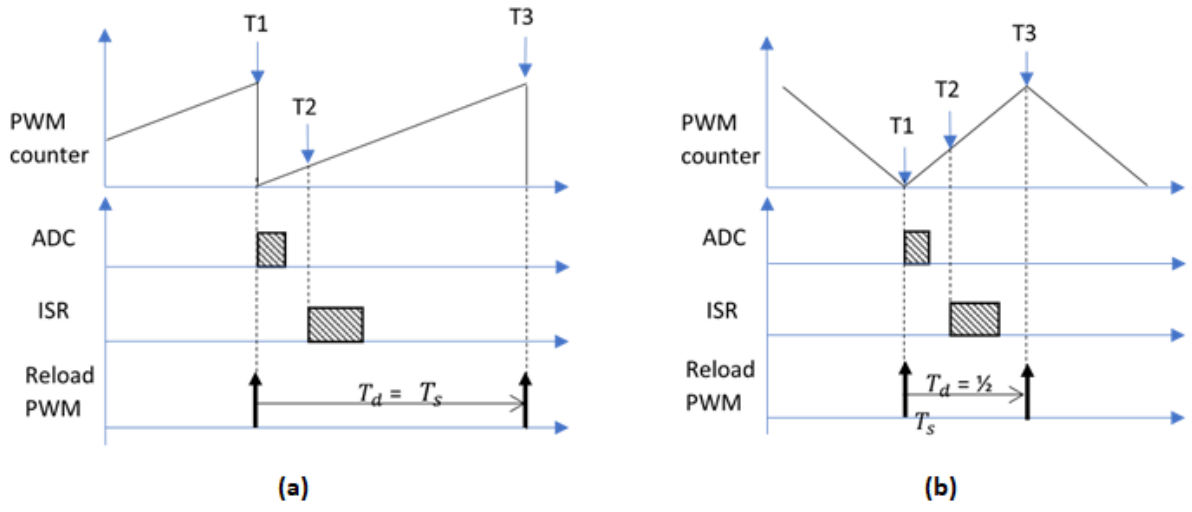

Figure 3. Minimum delay time is introduced by PWM adjusting: (a) up mode, (b) up-down mode. Source: Texas Instruments

Looking at Figure 4, T_d would be expressed as e^{-sxTd} in its transfer function, which would reduce the phase margin. Of course, when the phase margin is less than 45 degrees, the system will become unstable and oscillation will occur.

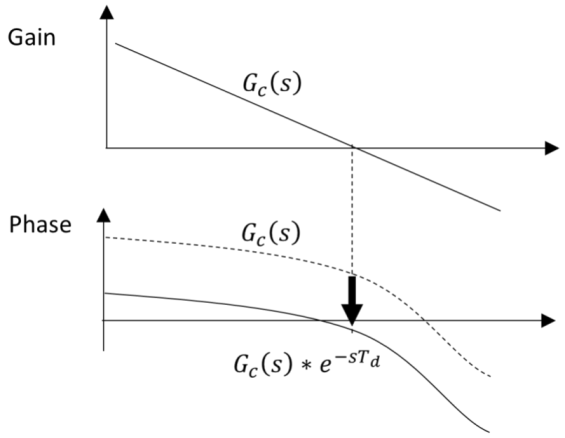

Figure 4. The influence of time delay is shown in the Bode plot. Source: Texas Instruments

A potential code mistake in digital control implementation

With correct execution, the minimum T_d is one switching cycle T_s half switching cycle $T_s/2$. But if you haven't considered the consequence of ADC, ISR and PWM reloading, it is possible that extending the control delay to more than one switching cycle may reduce phase margin and lead to instability.

For example, in Figure 5 the ADC's ISR trigger and PWM reload start at the same moment, when the PWM counter equals zero.

Although all blocks execute at the same time, can you expect T_d to be zero in this case? Absolutely not!

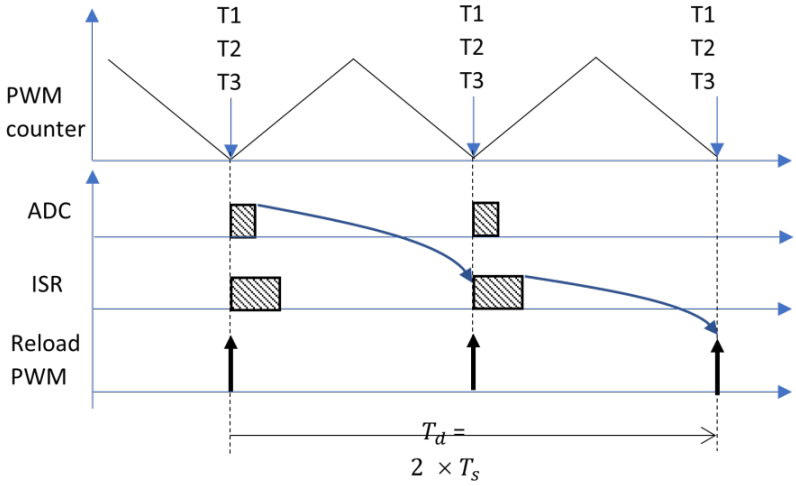

Figure 5. Here is an example of wrong code introducing a larger delay time. Source: Texas Instruments

This is because both the ADC conversion and ISR calculation require far more than one MCU clocking cycle - the ADC conversion still hasn't completed when the ISR reads the ADC result. Thus, the ISR will get the "old" sample value for calculating, and the calculation for the latest value is delayed until the next switching cycle. After the completion of the ISR calculation, the new PWM value is only written into the shadow register, which will be reloaded in the next switching cycle. In reality the total control delay of T_d will be two switching cycles, or $2 \times T_s$.

Besides the examples shown here, other implementations may introduce similar extended control delays - for example, if you put the ADC value reading after the controller calculation in the ISR code, or if you add an N-cycles algorithm average before calculating the controller.

As shown in Figure 6, when you set the GAIN cross frequency at around 3 kHz with the false implementation of Figure 5, the phase margin is 41.68 degrees. This is less than 45 degrees, and the choke current has significant oscillation, like the waveform of Figure 1, so you are forced to reduce the cross frequency to lower than 2 kHz; then the iTHD turns worse and fail the requirements.

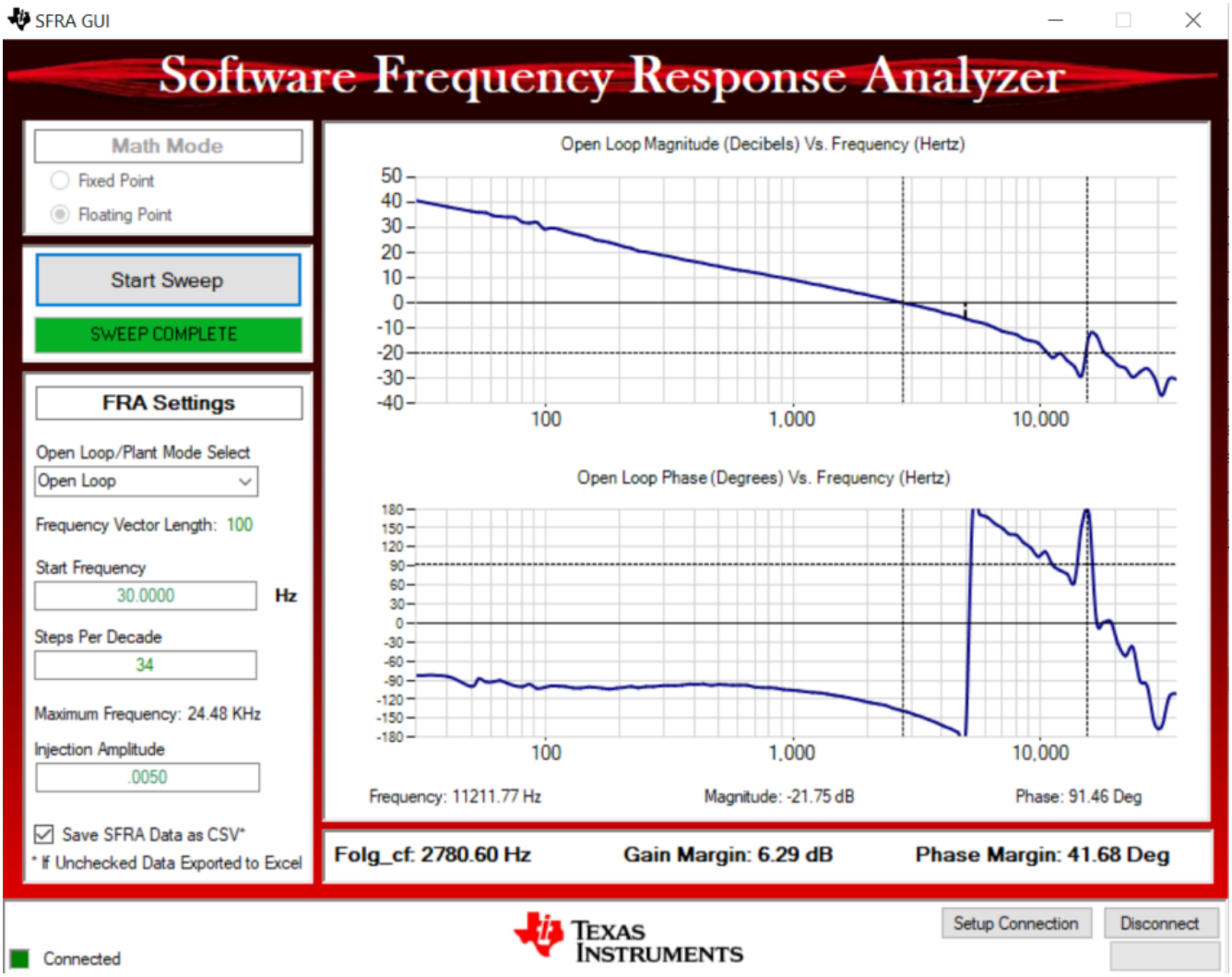

Figure 6. Bode plot with the wrong code implementation. Source: Texas Instruments

Design solution

You can easily fix this problem by moving the ADC conversion to the moment of counter = period and have PWM reloading occur in the next counter = period, as shown in Figure 7.

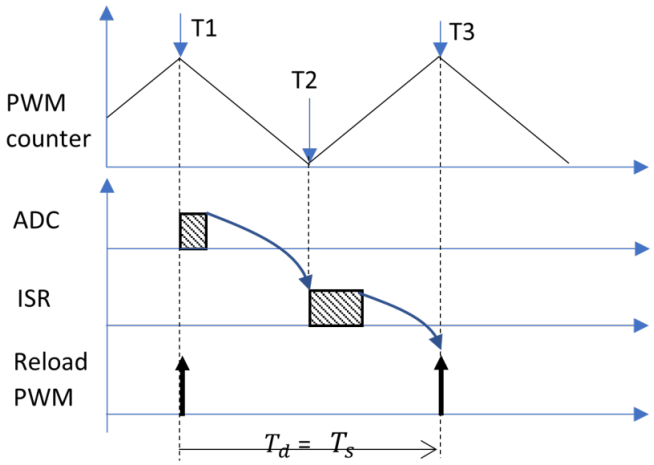

Figure 7. The control delay can be reduced with code improvement. Source: Texas Instruments

The control delay will be reduced to one switching cycle. The phase margin increases significantly, and the current oscillation disappears, as shown in Figure 8 and Figure 9.

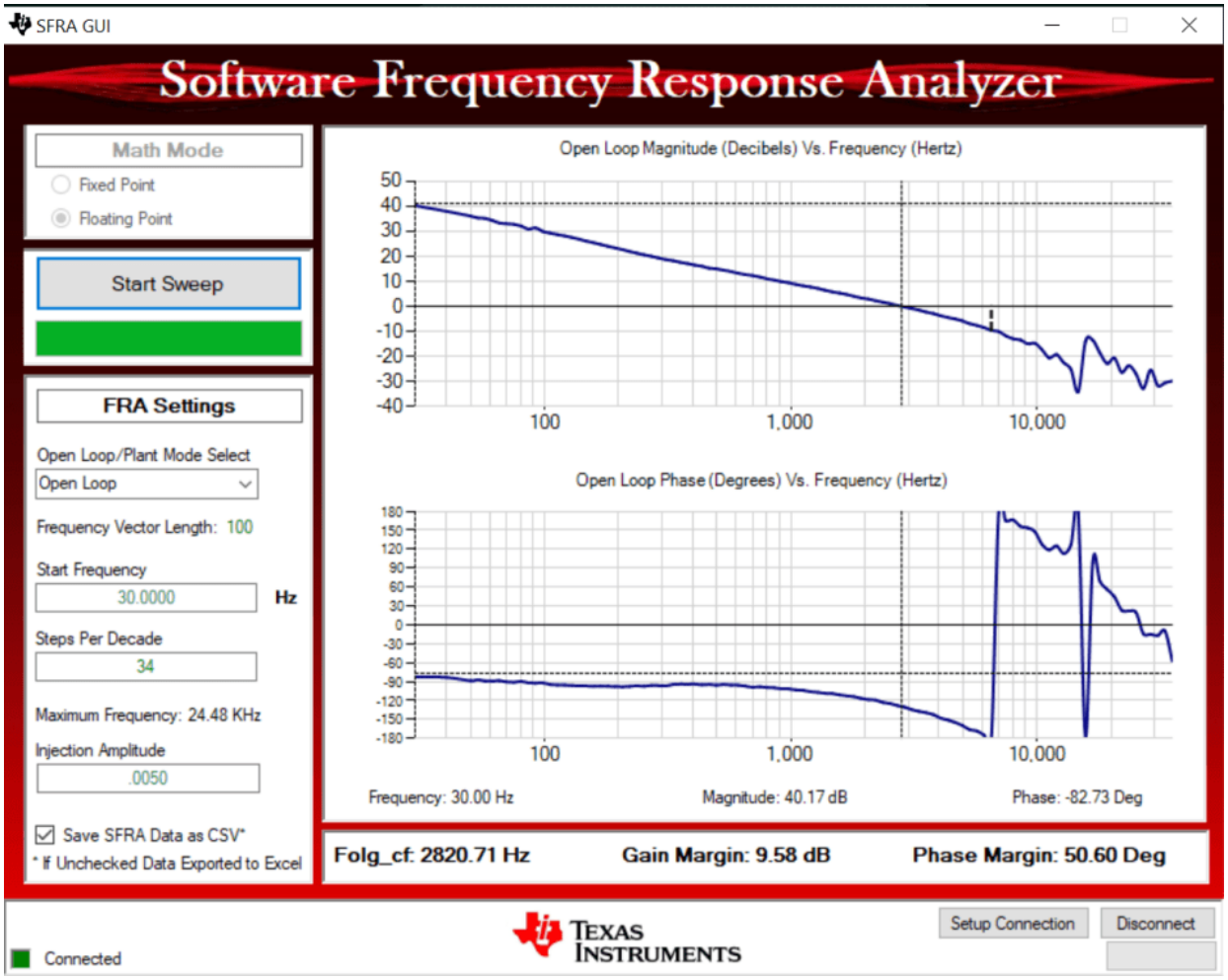

Figure 8. Bode plot with improved code. Source: Texas Instruments

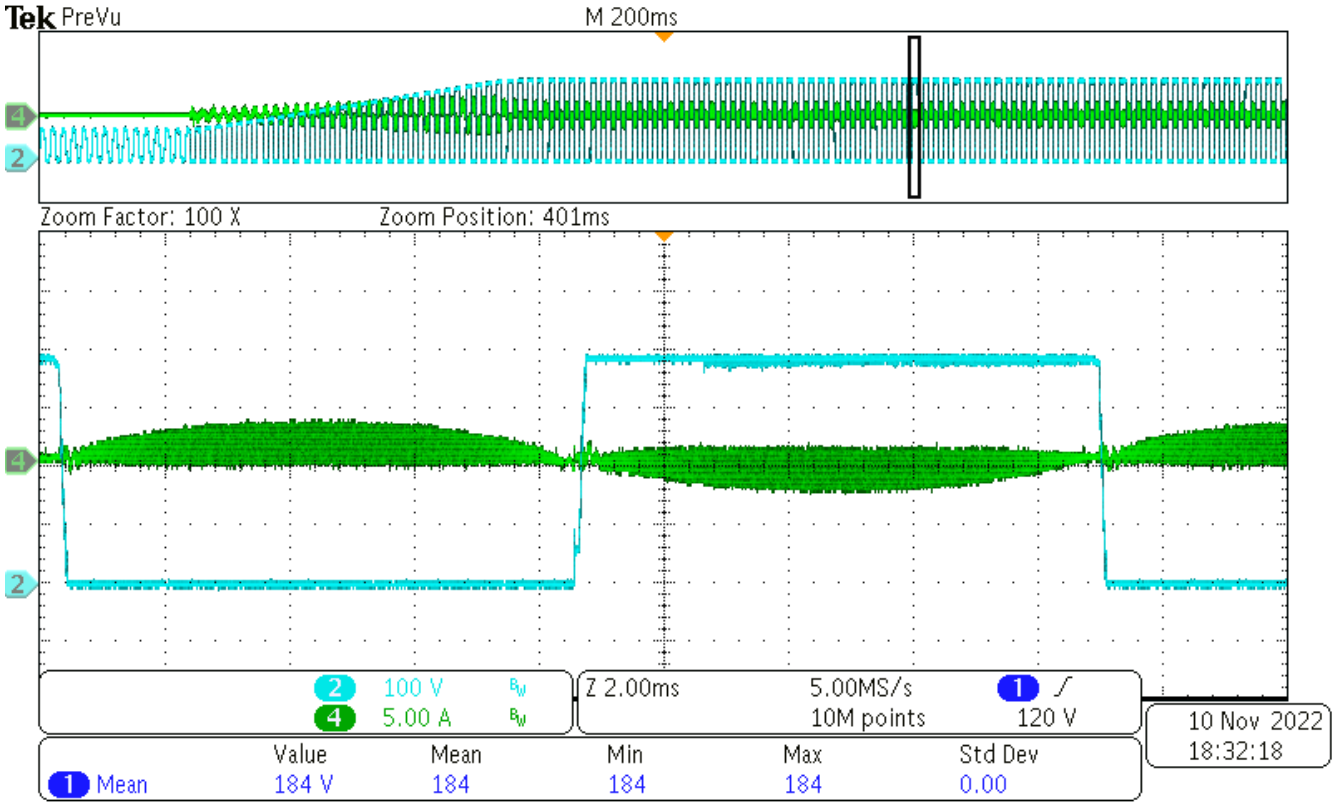

Figure 9. Waveform with improved code. Source: Texas Instruments

Well-organized control scheme

The control delay in a digital implementation, from ADC sampling to PWM adjustment, will reduce the phase margin and cause oscillation. When tackling this issue, consider the consequence of ADC sampling, controller calculation and PWM reloading. A well-organized control scheme can minimize the delay to one-half, or one switching cycle, which increases the phase margin and loop bandwidth.

Related Content

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- The basics of doing PID design: Part 1 – Classical control theory
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Technical Article

Use a thermal camera to assess temperatures in automotive environments

Josh Mandelcorn

Most electronics that go inside the car cabin need to be able to operate at up to 85°C without forced-air cooling. Product qualification requires showing that no component or trace on the board is getting too hot, even at maximum ambient temperatures. Existing methods of testing at elevated temperatures use thermocouples, which can be time-consuming and miss potential hot spots. Thermal cameras will pick up these missed spots and have become the best practice for room temperature tests. Room temperature testing will miss heating effects that only become noticeable in higher-temperature environments.

However, inserting a thermal camera into the 85°C chamber is not advisable as most such cameras cannot withstand above 70°C without damage. Pointing the thermal camera through the glass front of the thermal chamber also will not work, as the glass pane(s) distort the thermal image from the target device.

My proposed solution is to test the electronics in a convection thermal chamber with its door open, but covering the front with cardboard and tape, leaving only a small opening for the front of the thermal camera to get a good, clean thermal image. A thermocouple would be placed inside the chamber very close to the board under test to verify that the 85°C ambient has been achieved. The small opening for the thermal camera should not prevent this, and would allow the camera to be outside the chamber for the actual image.

I was able to find an old thermal chamber that only had heating coils below and no fan, relying only on convective airflow for heat transport (Figure 1). Furthermore, this oven did not have an interlock that shut off the coils when the front door was open. Using a newer oven, disconnecting the fan, and defeating the interlocks is another possibility, but not advised, as the manufacturers' warranty will be voided.

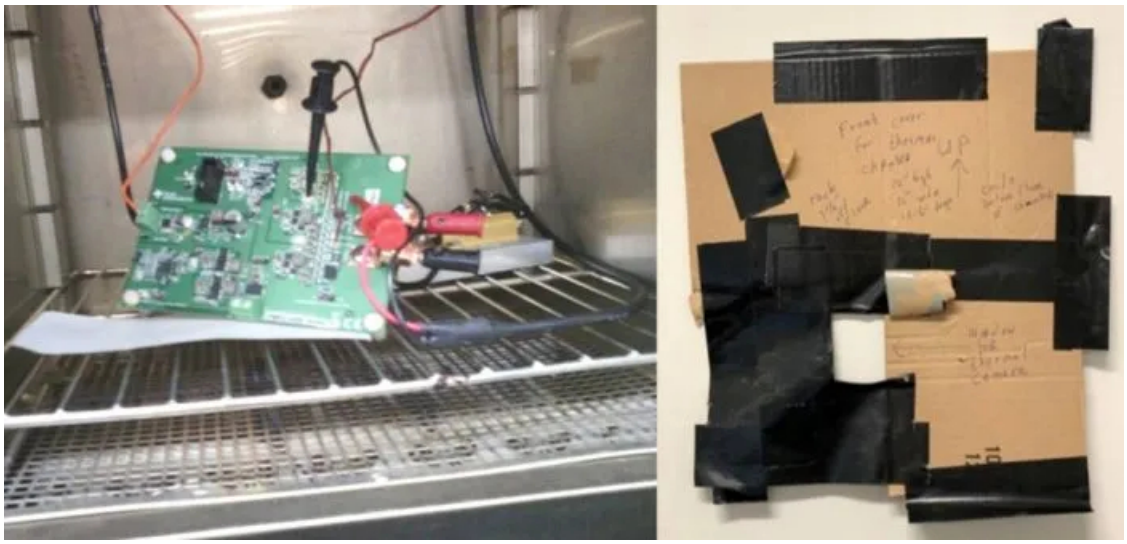

Figure 1. The setup includes the thermal chamber and the baffle

To the left of the board under test are the input 14-V power wires from an external lab power supply standing in for the car battery. To the right of board are load connections to resistors inside the chamber to load the 920 mV output with 22 A to represent the application load. Three monitoring wires can be seen for the thermocouple and output voltage sense (positive and negative); they went to multimeters to monitor temperature (Tektronix TX3) and output voltage (Fluke 87 III).

The Blue M DV-12A (“Gravity Oven”) thermal chamber was used with a front opening of 12 by 12 inches (and 12.5 inches deep), which was covered with the baffle (from Figure 1) during test. Similar ovens are generally available, offered in the several hundred dollar range. The square hole in the baffle was located to allow an external thermal camera (Flir E75) to focus on the hottest area on the board under test.

The board was powered with 14-V drawing, almost 2 A during the test, and the baffle cover was placed over the chamber opening. The thermal chamber coils were turned on and the setting adjusted to target 85-87°C on the thermocouple. The overall run took about 30 minutes with three thermal images taken, spaced five minutes apart, to verify that indeed thermal stabilization had been reached. Input current from the lab supply was also monitored to verify this stabilization. Current draw increased about 1% during run as expected due to increased conduction losses in the converters with increased temperature. Figure 2 shows the final thermal image.

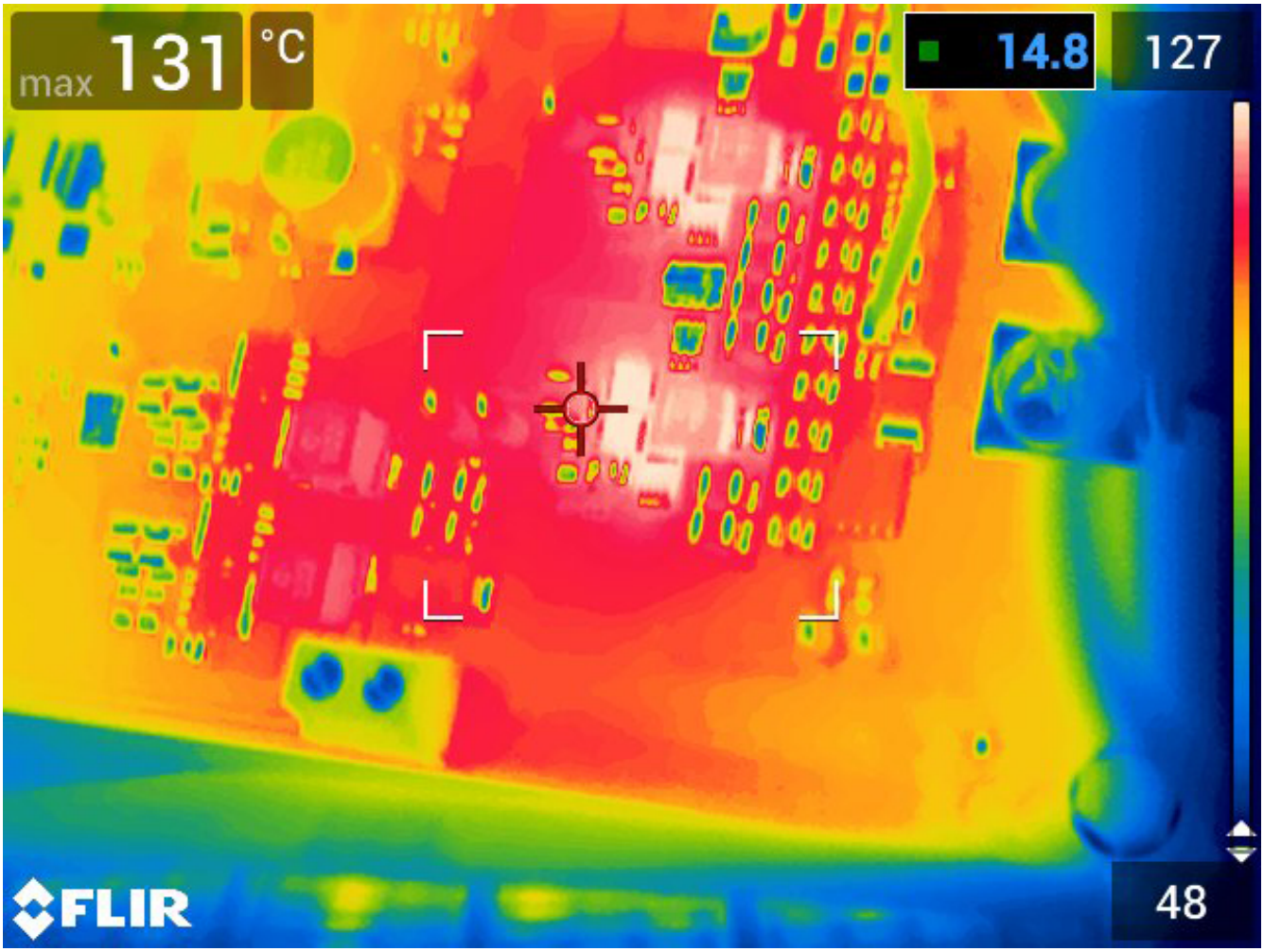

Figure 2. The final thermal image shows a max temperature of 131°C at the end of the run. Note the green thermocouple image to the right of the FETs

Output voltage monitored throughout the run stayed at 919 mV. Thermocouple readings varied between 85 and 88°C as the thermal chamber coils clicked on and off during the last 15-20 minutes of the run. Repeated thermal images over a nine-minute span with the same max temperature verified that thermal stabilization was achieved.

To verify ambient temperature monitoring, a run was done with two thermocouples monitoring the ambient; one as shown in Figure 2 and one slightly below the board. Both monitors read within 1°C of each other. As an additional verification, the run was repeated with a thermocouple glued on the hottest FET, and its max temperature was 4-5°C cooler than what the thermal camera picked up. This also demonstrates that the thermal camera will pick up hot spots missed by the thermocouples.

Overall, this demonstrated a more thorough method of high ambient thermal verification for automotive applications at moderate incremental cost (assuming existing availability of a thermal camera). This method will pick up thermal runaway situations that earlier methods have missed. If a used convection oven needs to be purchased, the savings from not having to glue multiple thermocouples will quickly cover the cost.

Related articles

- Thermocouples: Basic principles and design essentials
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- Book review: A guide to sensors in automotive
- Thermocouples: Simple but misunderstood
- Minimize measurement errors in RTD circuits
- Clever techniques improve thermocouple measurements

Technical Article

How to latch off a power converter that has a hiccup fault response

Pradeep Shenoy

Power converters are typically designed to protect against unwanted fault scenarios. For example, if too much current is being drawn on the converter output, overcurrent protection may engage. This is helpful if the converter's output terminals are accidentally shorted together or if the load current goes above the designed maximum current. Other common fault situations include exceeding the thermal shutdown trip point (overheating) and the output voltage going out of bounds (overvoltage or undervoltage).

A popular way to respond to faults is called a hiccup. The power converter will turn itself off, wait for some time (30 ms, for example) and then automatically restart itself. Figure 1 shows an example of this response, measuring both the output voltage and inductor current. A hiccup fault response gives the system a chance to recover without external intervention. It also helps reduce the power consumed and heat generated in the case of shorted outputs.

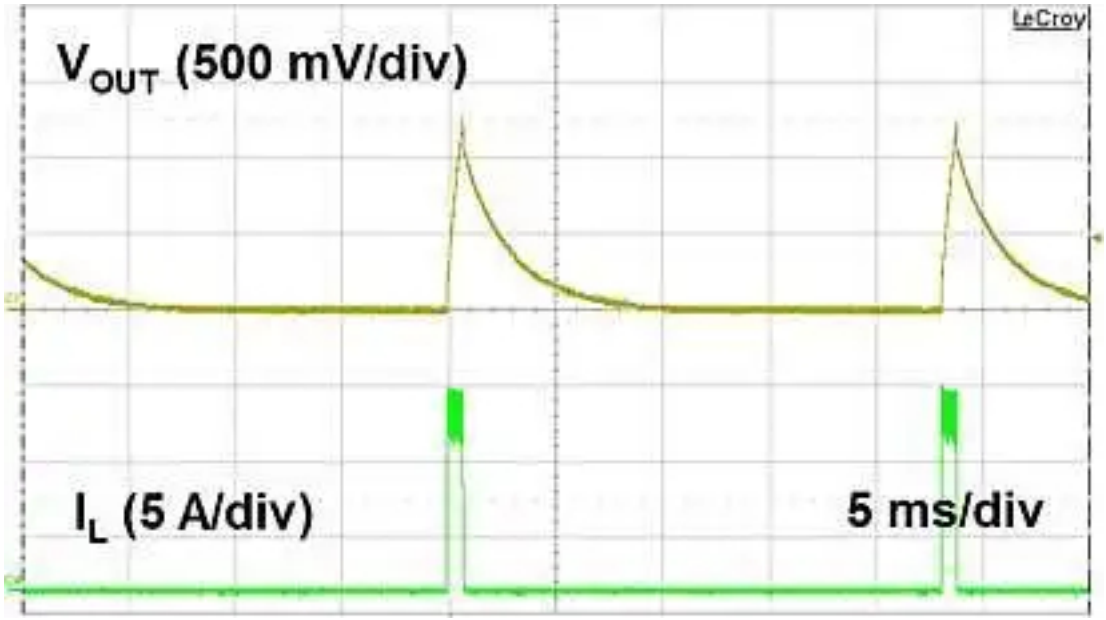
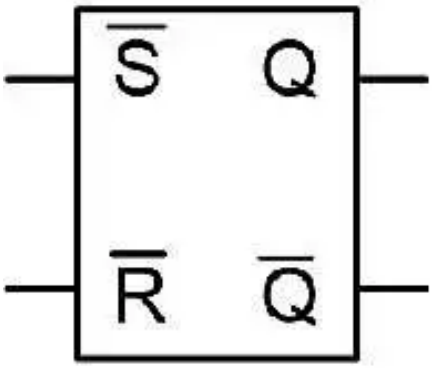


Figure 1. Hiccup fault response caused by an overcurrent scenario.

There are times when a hiccup response is not wanted. Perhaps you want a central controller to manage the fault response in a more complex or sophisticated manner. Some systems have redundancy built in and want to completely turn off the faulting subsystems in order to ensure that they do not interfere with functioning subsystems. In these cases, the desired fault response may be to latch off the faulting power converters. Latching off the power converter will prevent it from restarting unless the enable (EN) pin or supply voltage is cycled to reset the latch. Some devices, like the TPS53511, have a built-in latch-off response, but most do not.

It is possible to add a latch-off fault response to a power converter with a simple set/reset (SR) latch circuit. Figure 2 shows an SR latch and its truth table. For this example, the SR latch has active-low inputs. This means that when the inputs are high, the outputs Q and Q-Bar do not change. If the set input goes low, Q will be set high (1). If reset goes low, Q will be low (0). If both inputs are low, the outputs are in an undetermined state, a situation that generally should be avoided. Additional logic gates can overcome this situation.



$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
1	1	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
0	0	X	X

Figure 2. SR latch with active-low inputs and corresponding truth table.

Figure 2 illustrates a high-level approach to implementing the latch circuit. Many power converters and monitoring circuits have a power good (PGOOD) output. If there is a fault in the converter, the PGOOD signal will pull low, indicating that the converter has a problem. When the PGOOD signal goes low, the output of the latch circuit (Q) will go high, which in turn will pull the EN pin of the converter low. The converter will turn off when the EN pin goes low and will not restart by itself. A reset signal sent to the latch restarts the converter and brings the Q output low, which in turn brings the EN pin high. The inverters are included to make interfacing simpler; they are implemented with an open-drain metal-oxide semiconductor field-effect transistor (MOSFET).

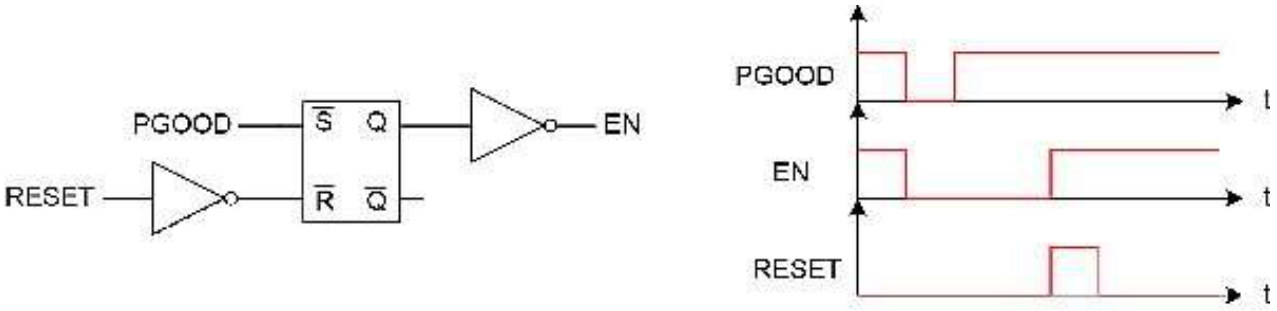
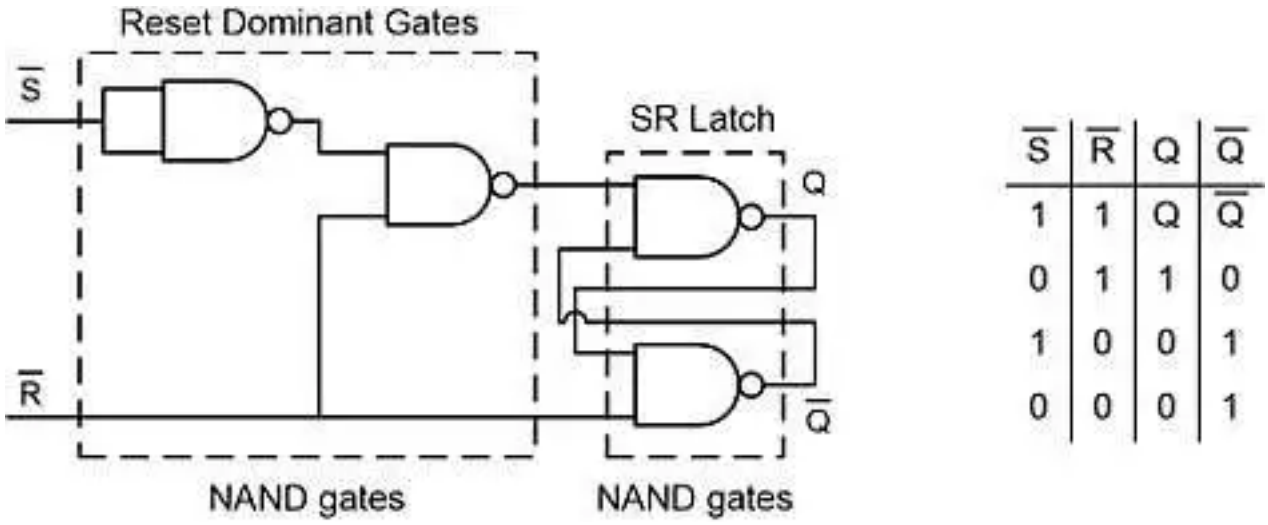


Figure 3. Latch circuit overview and example signal diagram.

You want to ensure that the converter can correctly start up or restart even while the PGOOD signal is low; thus, you need the latch circuit to be reset-dominant. In other words, when both the set and reset inputs are low, the reset input will dominate, resulting in the Q output being low. Figure 4 shows a simplified implementation using only NAND gates, with the corresponding truth table. It is possible to create this circuit with two dual NAND gate SN74AUP2G00 integrated circuits (ICs) or one quad NAND gate SN74HC00 IC.



$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
1	1	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
0	0	0	1

Figure 4. Reset-dominant latch circuit using NAND gates and corresponding truth table.

Figure 4 shows the overall implementation of the latch-off circuit. The PGOOD pin of the power converter pulls high using an external resistor (to 3.3 V). Whenever a fault occurs, the open-drain MOSFET connected to PGOOD will pull the S-bar input to latch low. The Q output then goes high, which turns on MOSFET S1. The EN pin pulls low, which turns the converter off and prevents hiccup auto-restart. When the converter input voltage rail (PVIN) ramps up, capacitive coupling through the parasitic gate-to-drain capacitance (C_{gd}) could pull up on the gate of S1 and turn it on. A pulldown resistor on the gate of S1 may be helpful to ensure that S1 does not inadvertently turn on.

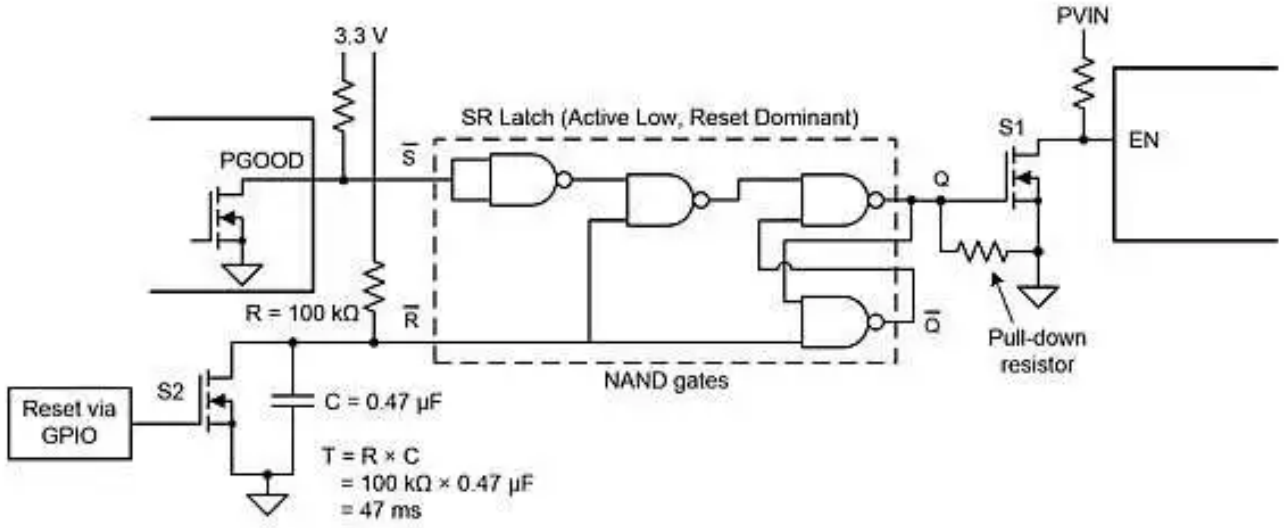


Figure 5. Resettable latch-off circuit.

The R-Bar input to the SR latch is pulled high through a 100-kΩ resistor. The open-drain MOSFET S2 can pull the R-Bar signal low whenever a reset signal is provided to the gate of S2. A capacitor (C, connected in parallel with S2) forms a delay circuit with pullup resistor R. The RC time constant of the delay is about 47 ms in this example. This delay is adjustable to ensure that the R-Bar input stays low during startup. The slow edge rate on the R-Bar can damage the inputs of the some complementary metal-oxide semiconductor (CMOS) NAND gates caused by excessive current draw. The SN74AUP2G00 gates will not be damaged by this, however, because they have relatively weak drivers.

Another approach is to either use Schmitt-trigger input NAND gates or add a Schmitt-trigger buffer at the R-Bar input. In a third option, the switch S2 can be continuously turned on to pull R-Bar low during startup, and the RC delay could be reduced or entirely removed by adjusting the R and C values.

It is possible to use the circuit described here in a wide variety of power-converter applications that require a latch-off fault response. The latch-off circuit uses a few simple components and logic gates to achieve a flexible, reliable solution.

Related articles

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Technical Article

Think outside the LLC series resonant converter box

Sheng-Yang Yu

For over a decade, power-supply industries have widely applied the inductor-inductor-capacitor (LLC) series resonant converter (LLC-SRC) shown in Figure 1 with two resonant inductors (two “Ls”: L_m and L_r) and one resonant capacitor (one “C”: C_r) as a low-cost, high-efficiency isolated power stage. An LLC-SRC has a soft-switching nature without a complicated control scheme. Its soft-switching feature enables the use of components with lower voltage ratings and also provides high converter efficiency. Its simple control scheme – variable frequency modulation with a fixed 50% duty cycle – requires a lower controller cost when compared to controllers used for other soft-switching topologies, like phase-shift full-bridge converters.

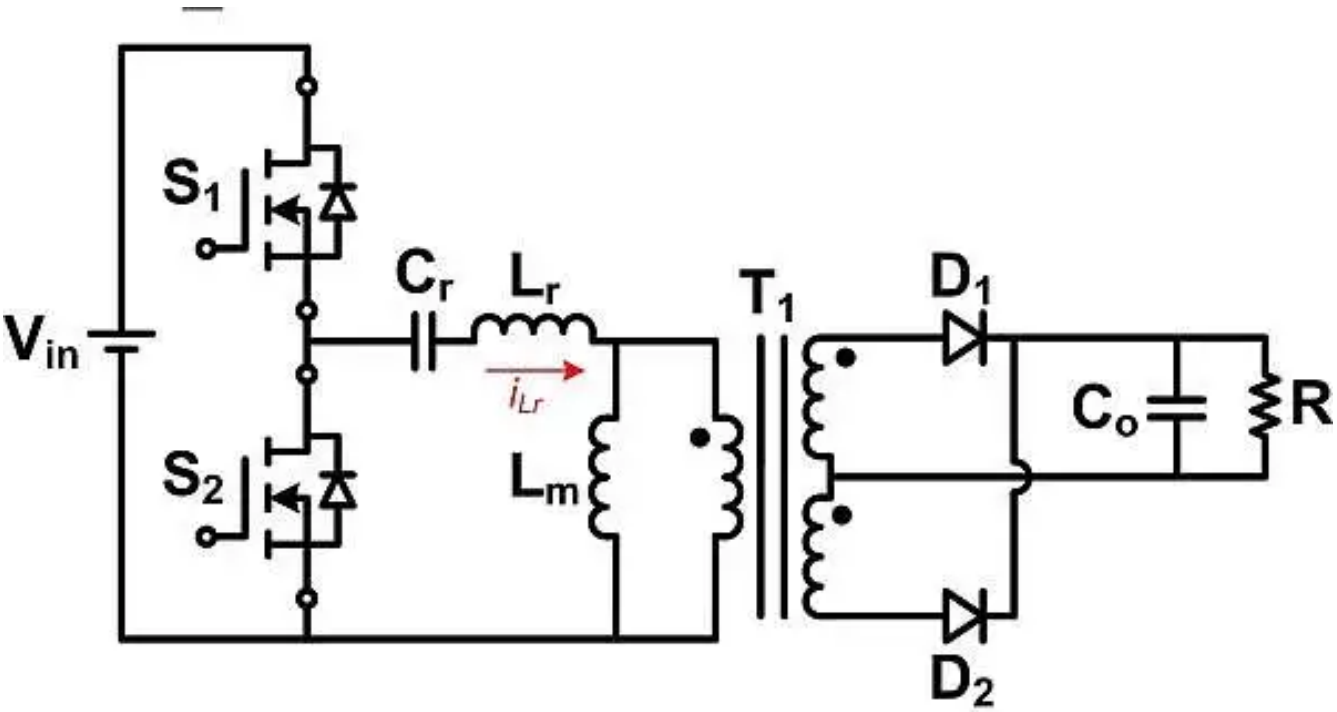

Figure 1. An LLC-SRC

Although an LLC-SRC can achieve much higher efficiency than hard-switching flyback and forward converters, there are still a couple of design challenges if you want to achieve the best efficiency. First, the ratio of two resonant inductors – L_m-to-L_r – will probably have to be smaller than 10 in an LLC-SRC design in order to allow a wide-enough controllable range. At the same time, you’ll need a large inductance on L_m to lower the circulating current – which implies that you’ll need to keep the L_r inductance large to keep the resonant inductor ratio low.

It’s interesting to note that the current in a series resonant inductor L_r is fully AC without any DC content – which means high magnetic flux density variations (ΔB is high). High ΔB means high AC-related inductor losses. If the inductor is wound on a ferrite-based core, you’ll have a high winding loss from the fringing effect near the air gap of the core.

A large inductance on L_r means more turns on the inductor and higher AC winding losses. That is why many LLC-SRC designs apply a powder-iron-based core to the resonant inductor as a trade-off between winding loss and core loss. Nevertheless, high ΔB generates considerable losses on the resonant inductor – either a high winding loss or a high core loss.

A second challenge in an LLC-SRC design is how to best optimize synchronous rectifier (SR) control. LLC-SRC rectifier current-conduction timing depends on the load condition and the switching frequency. The most promising method for LLC-SRC SR control is to sense the SR field-effect transistor (FET) drain-to-source voltage (V_{DS}) and turn the SR on and off when V_{DS} is below or above certain levels. The V_{DS} sensing method requires millivolt levels of accuracy, and therefore can only be realized in an integrated circuit. Self-driven or other low-cost SR control schemes are not applicable to LLC-SRCs because of their current-fed capacitor-loaded output configuration. Thus, the cost of an LLC-SRC SR controller circuit is generally higher than it is for other topologies.

To address these two challenges – high inductor losses and SR control – and yet still harness most of the benefits that a resonant converter can provide, consider using a modified CLL multiresonant converter (CLL-MRC), shown in Figure 2.

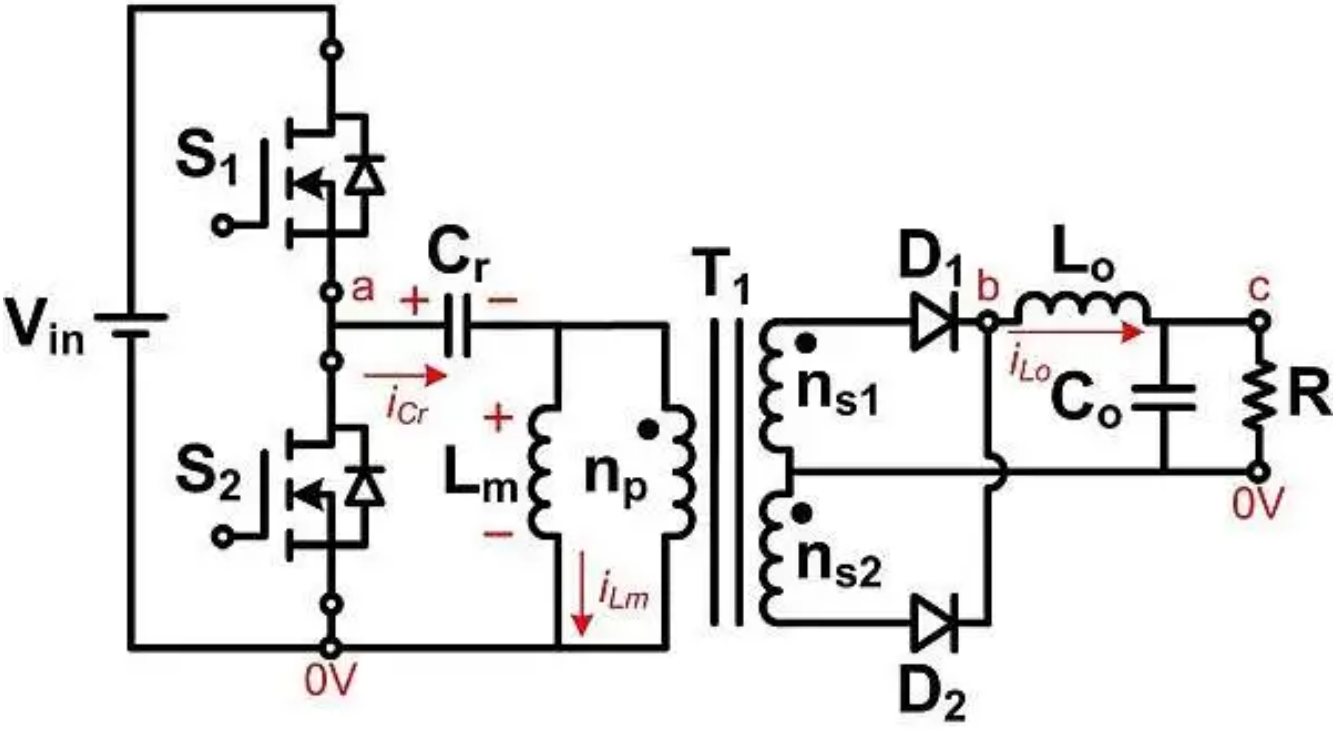

Figure 2. A modified CLL-MRC

Unlike a CLL-MRC, where all three resonant elements (one capacitor and two inductors) are on the input side, a modified CLL-MRC moves one inductor from the input side to the output side and has the inductor placed after the rectifier – L_o, as shown in Figure 2. This modification allows DC current content on the resonant inductor, which implies less ΔB and possibly lower magnetic losses.

Figure 3 illustrates the operation of the modified CLL-MRC, where f_{sw} is the converter switching frequency and $f_{r1} = \{2\pi[C_r (L_{r1} // L_{r2})]^{0.5}\}^{-1}$ is one of the two resonant frequencies. When f_{sw} is lower than f_{r1}, the output winding current drops to zero before the end of a switching period, just like the output winding current in an LLC-SRC. Now you have an inductor at the output. A simple capacitor and resistor set can sense the output inductor voltage. Every time a large rate of voltage change (dV/dt) occurs, it is the timing to turn the SRs on or off. Hence, the SR control scheme costs less than the V_{DS} sensing scheme.

When f_{sw} is higher than f_{r1}, the output inductor current operates in continuous conduction mode. In other words, ΔB becomes less, the inductor AC losses can be much smaller, and the converter efficiency is possibly higher than in an LLC-SRC.

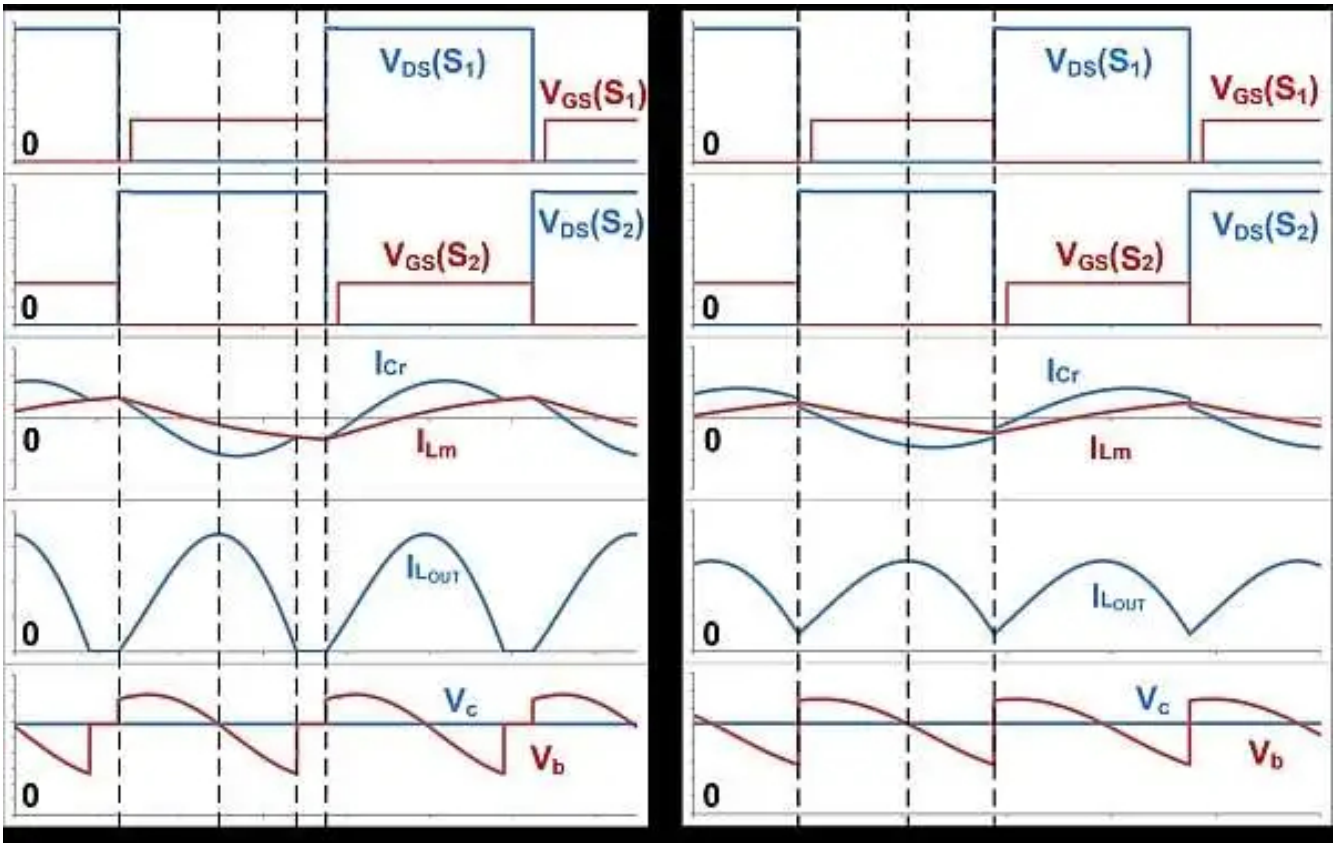

Figure 3. Modified CLL-MRC key waveforms: $f_{sw} < f_{r1}$ (left); $f_{sw} > f_{r1}$ (right)

To verify these performance assumptions, I have built an LLC-SRC and a modified CLL-MRC power stage with the exact same components and parameters. The only difference is the application of a 72µH inductor as the LLC-SRC resonant inductor and a 1µH inductor as the modified CLL-MRC output inductor.

Figure 4 shows the efficiency measurements of both power stages. With a lower input voltage, f_{sw} is less than f_{r1} – thus the L_o current in the modified CLL-MRC is still in discontinuous conduction mode with large ΔB. Therefore, there isn't an efficiency benefit on the modified CLL-MRC in this operational condition.

When the input voltage goes higher, f_{sw} is higher than f_{r1} and the L_o current is in continuous conduction mode. With a 430-V input, the modified CLL-MRC's efficiency is 1% higher than the LLC-SRC. This comparison shows that if you design the modified CLL-MRC to always operate in a frequency higher than f_{r1}, its efficiency performance can be better than an LLC-SRC over the entire range.

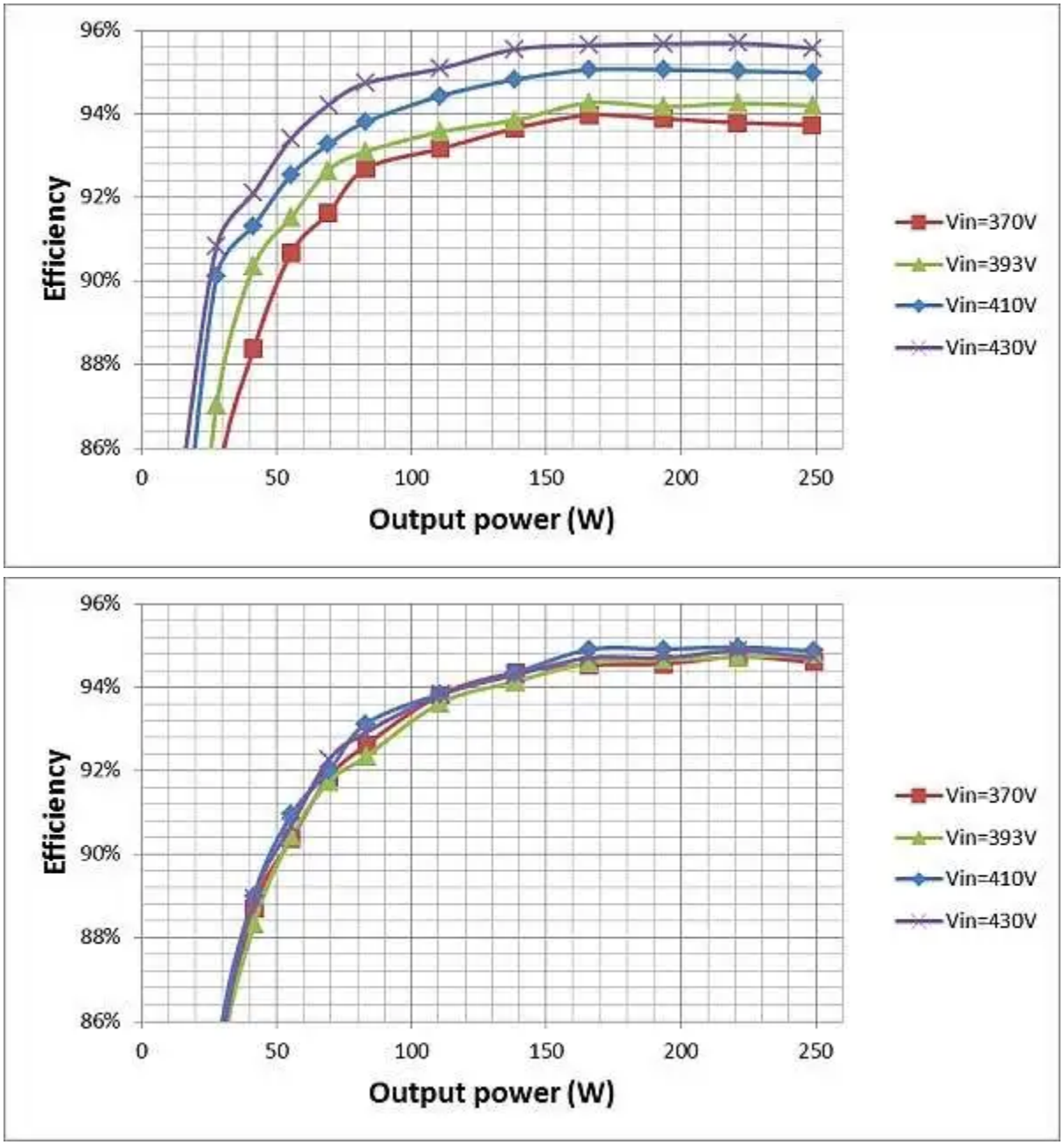

Figure 4. Converter efficiencies with different input voltage levels: modified (top) CLL-MRC; LLC-SRC (bottom)

An LLC-SRC is indeed a good topology and provides many attractive features. But depending on the application, it might not be the best solution. From time to time, you need to think outside the box to achieve better efficiency with a lower circuit cost.

Additional resources

- Read these papers from Texas Instruments Power Supply Design Seminar:
  - "Designing an LLC Resonant Half-Bridge Power Converter."
  - "Survey of Resonant Converter Topologies."
  - "Control and Design Challenges of Synchronous Rectifiers."
- Check out the 400VDC Input to 28V/9A Output Compact, High Efficiency CLL Resonant Converter Reference Design.

Related articles

- LLC resonant topology lowers switching losses, boosts efficiency
- High efficiency resonant mode implementation using digital control
- Design considerations when selecting half bridge resonant LLC converters and primary side MOSFETs
- Using quasi-resonant and resonant converters
- Power Tips #77: Designing a CCM flyback converter

Technical Article

Five major trends in power-supply designs for servers

Richard Yin

Because servers are essential for handling data communications, the server industry has grown exponentially in parallel with the internet. Although server units were originally based on a PC architecture, a server system must be able to handle the increasing number and complexity of network hosts.

Figure 1 shows a typical rack server system in a data center and a block diagram of a server system. Power-supply units (PSUs) are at the heart of a server system and require a complex system architecture. This article will examine five server PSU design trends: power budget, redundancy, efficiency, operating temperature, and communication and control.

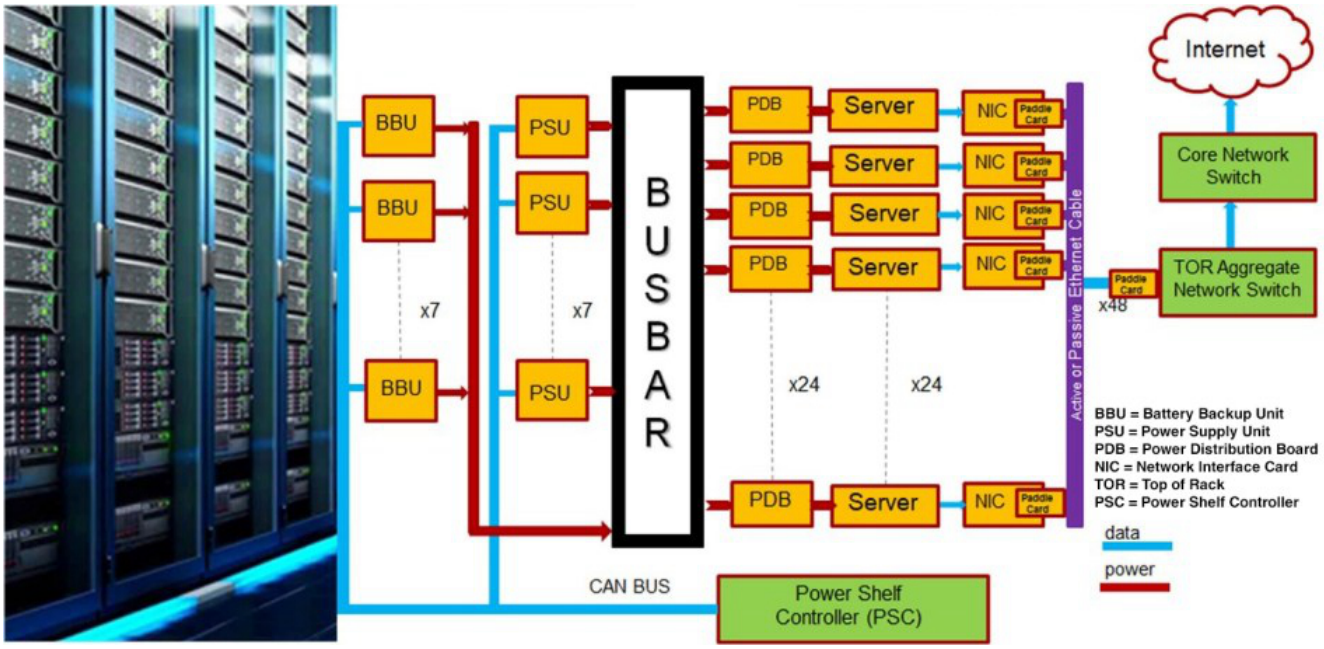

Figure 1. A server system block diagram along with how a server is positioned in a data center. Source: Texas Instruments

Trend No. 1: Power budget

In the early 21st century, the power budget of a rack or blade server PSU was in the 200-W to 300-W range. At that time, power consumption per central processing unit (CPU) was in the 30-W to 50-W range. Figure 2 shows CPU power consumption trends.

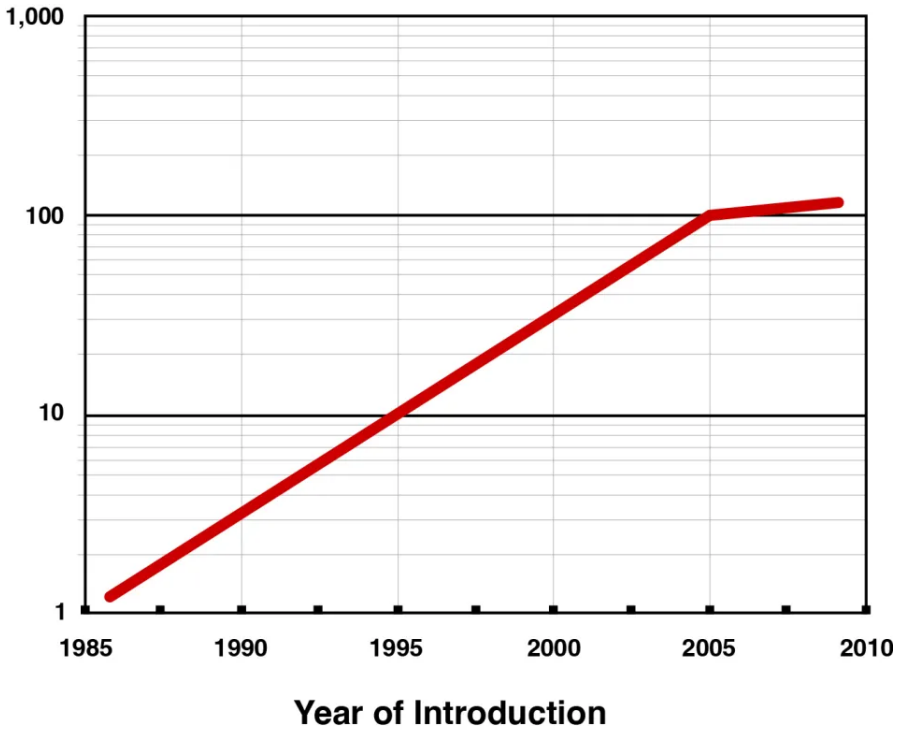

Figure 2. The CPU power consumption trends for the early 21st century.

Today, a server CPU's power consumption is around 200 W—with thermal design power closed to 300 W - greatly increasing the server PSU's power budget to a range of 800 W to 2,000 W. In order to support more and more server computation requirements such as cloud computing and artificial intelligence (AI) calculations on the internet, servers can include graphics processing units (GPUs) to work alongside CPUs. This inclusion could increase a server's power demand beyond 3,000 W within five years. However, since most rack or blade server PSUs are still using an AC inlet with up to a 16-A current rating, they will have limited power budgets: around 3,600 W at a 240 V_{AC} input, accounting for converter efficiency. So 3,600 W will still be a server rack PSU's power limit in the near term.

For the data center power shelf, server PSU designers widely apply the International Electrotechnical Commission (IEC) 60320 C20 AC inlet with 20-A current rating. PSU power budgets are limited by their AC inlet current rating, which allows about 3,000 W in today's data center PSUs; but in the near future, a data center PSU's power level could increase to over 5,000 W. To allow a higher power budget per PSU and achieve higher power density, you can also use a busbar for the AC inlet to increase the input current rating.

Trend No. 2: Redundancy

The importance of reliability and availability in a server system necessitates redundant PSUs. If one or more PSUs fail, other PSUs in the system can take over to deliver energy.

A simple server system can have 1+1 redundancy, meaning that there is one active PSU and one redundant PSU in the system. A complex server system might have an N+1 or N+N (N>2) redundancy, depending on system reliability and cost considerations. In order to keep the system operating normally when a PSU needs to be replaced, the system needs a hot-swap (ORing control) technique. And because multiple PSUs deliver power simultaneously in an N+1 or N+N system, server PSUs also require a current-sharing technique.

Even a PSU in standby mode - not delivering power to the output from its main power rail - still requires instant delivery of full power after a hot-swap event, thus requiring constant activation of the power stage. In order to reduce the power consumption of the redundant power supply in standby mode, "cold redundancy" functionality is becoming a trend. The purpose of cold redundancy is to shut down the main power operation or operate in burst mode, enabling the redundant PSU to minimize standby power consumption.

Trend No. 3: Efficiency

Efficiency specifications in the early 2000s were just above 65%; at the time, server PSU designers did not prioritize efficiency. Traditional converter topologies could easily satisfy the 65% efficiency target. But because a server needs to operate continuously, higher efficiency can greatly reduce total cost of ownership.

Since 2004, the 80 Plus standard has provided certifications for PC and server PSU systems that can achieve over 80% efficiency. Server PSUs in mass production today mostly achieve the 80 Plus Gold (>92% efficiency) requirement, and some can even achieve 80 Plus Platinum (>94% efficiency).

Server PSUs under development today mainly target the even higher 80 Plus Titanium specifications, which require over 96% peak efficiency at half loads. Table 1 shows the various 80 Plus specifications.

Table 1. The 80 Plus specification ensures above 80% efficiency.

230 V internal redundant	10%	20%	50%	100%
80 Plus				
80 Plus Bronze		81%	85%	81%
80 Plus Silver		85%	89%	85%
80 Plus Gold		88%	92%	88%
80 Plus Platinum		90%	94%	91%
80 Plus Titanium	90%	94%	96%	91%

Also, according to the Open Compute Project (OCP) open-rack specification that data center PSUs are following, a PSU needs to achieve over 97.5% peak efficiency. Therefore, new topologies such as bridgeless power factor correction (PFC) and soft-switching converters, along with wide bandgap technologies such as silicon carbide (SiC) and gallium nitride (GaN), can help PSUs achieve 80 Plus Titanium and open-compute efficiency goals.

Trend No. 4: Operating temperature

In the context of server PSU thermal management, designers define the ambient temperature at the PSU AC inlet where the fan is located as the server PSU operating temperature. The operating temperature started at 45°C maximum in the early 2000s and today reaches 55°C maximum, depending on the cooling system in the server room.

A higher operating temperature reduces the energy costs of a server cooling system. Compared to the capital expenditures of a data center (such as hardware equipment), energy costs as an operating expense are expected to be higher than capital expenditures over time. According to the power usage effectiveness (PUE) standard:

PUE = Total Datacenter Power/Actual IT Power

As shown in Table 2, a lower PUE number means an efficient data center. Figure 3 is an estimation of the PUE number under different operating temperatures. For example, a data center with a PUE of 1.25 can only allow 10% of overall power consumption on its cooling system. This implies the need for a higher operating temperature in a server PSU.

Table 2. A lower PUE number translates into an efficient data center.

PUE	Level of Efficiency
1.25	Very Efficient
1.5	Efficient
2	Average
2.5	Inefficient
3	Very Inefficient

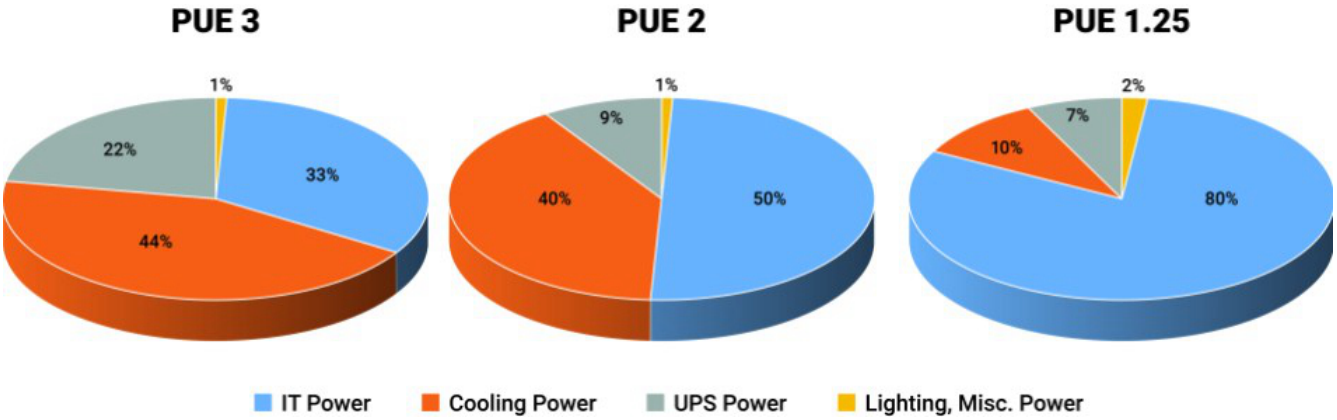

Figure 3. An estimation of the PUE number under different operating temperatures shows reduced cooling costs with a higher operating temperature.

Trend No. 5 Communication and control

Communication and control have played an important role in server power over the years. In the early 2000s, the PSU's internal information was transmitted to the system side through the System Management Bus interface. In 2007, the Power Management Bus (PMBus) interface added functions, including configuration, control, monitoring and fault management, input/output current and power, board temperatures, fan speed control, real-time update code, overvoltage (current, temperature), and protection. Then, in response to increased demand for data center power shelves, the Controller Area Network (CAN) bus became a part of server power communication.

Power-management controllers have also evolved along with the communication bus. In the early 2000s, analog controllers mainly controlled server PSUs. As more and more control demands increased the need for communication, it became easier to realize those demands with digital controllers. Using digital control also reduces a hardware engineer's debugging efforts, potentially reducing labor costs during the PSU design and verification stages.

Future development trends for server PSUs

As server power budgets grow while the volume remains fixed, power density requirements will become stricter. Power density has increased from single digits at the beginning of the 2000s to nearly 100 W/in^3 on newly developed server PSUs. Improving converter efficiency through topology and component technology evolutions is the solution to achieving high power density.

As was the case with the current, power and efficiency trends, the ideal diode/ORing controller needs to deliver high current in a small package. The ideal diode/ORing controller must also integrate features such as monitoring, fault handling and transient handling to reduce the overall component count and PCB area needed to achieve these functionalities.

For example, a PFC circuit in a server PSU has evolved from passive PFC to active-bridge PFC to active bridgeless PFC. Isolated DC/DC converters have evolved from hard-switching flyback and forward converters to soft-switching inductor-inductor-capacitor resonant and phase-shifted full-bridge converters. Nonisolated DC/DC converters have evolved from linear regulator and magnetic amplifiers to buck converters with synchronous rectifiers. Subsequent increases in overall efficiency reduce internal power consumption and the effort required to resolve thermal issues.

Component technologies applied to server PSUs have also evolved, from IGBTs and silicon MOSFETs to wide bandgap devices such as silicon-carbide MOSFETs and gallium-nitride FETs. The nonideal switching characteristics of IGBTs and silicon MOSFETs limit the switching frequencies below 200 kHz. While wide bandgap devices have switching characteristics closer to ideal switches, using wide bandgap devices can enable higher switching frequencies to help shrink the number of magnetic components used in the PSU.

As the operating temperature increases, components in a server PSU need to handle higher thermal stress, which also drives circuit evolution. For instance, a conventional implementation applies a mechanical relay in parallel with a resistor to suppress the input in-rush current during startup. But because of their bulky size, reliability concerns and lower temperature rating, solid-state relays are now replacing mechanical relays in server PSUs.

The 3.6-kW single-phase totem-pole bridgeless PFC design with >180-W/in^3 power density and 3-kW phase-shifted full bridge with active clamp design with >270-W/in^3 power density aim to meet common redundant power-supply specifications in servers (Figure 4).

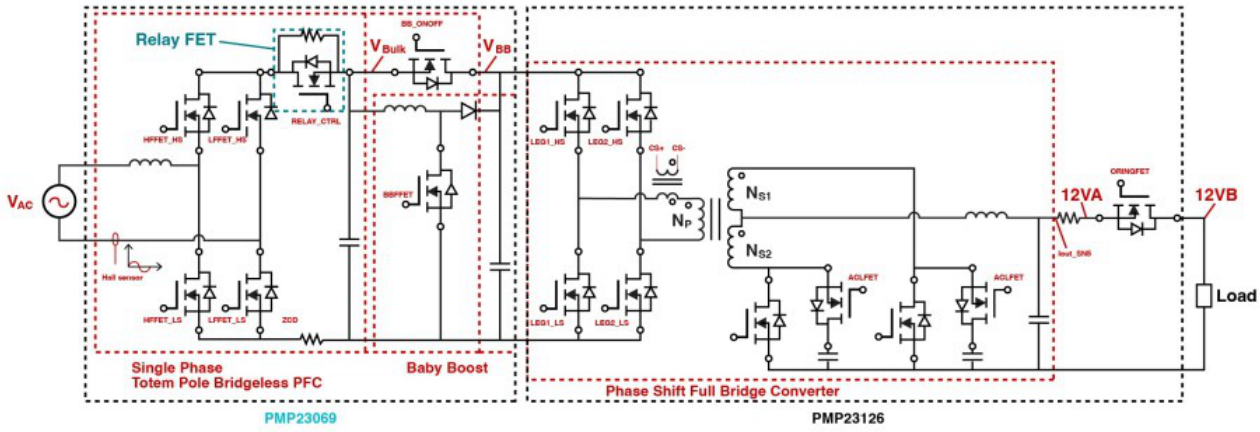

Figure 4. The block diagram shows the 3.6-kW and 3-kW reference designs. Source: Texas Instruments

In the 3.6-kW PFC design, a solid-state relay accommodates a high operating temperature. Here, the LMG3522R030 GaN FET enables the use of a bridgeless totem-pole PFC topology. A “baby boost” reduces the bulk capacitor volume for higher power density.

In the 3-kW phase-shifted full-bridge design, the LMG3522R030 GaN FET helps lower the circulating current and makes it possible to achieve soft switching. An active clamping circuit acting as a lossless snubber enables higher converter efficiency with lower synchronous rectifier voltage stresses. All the aforementioned control requirements are achieved through C2000™ microcontroller acting as digital control processor.

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Technical Article

How an upside-down buck offers a topology alternative to the non-isolated flyback

John Dorosa

One of the most common sources of power is offline, also known as the AC mains. With the increase of products aimed at integrating typical household features, there is greater demand for low-power offline converters that require less than 1W of output capability. For these applications, the most critical design aspects are efficiency, integration, and low cost.

When deciding on a topology, the flyback is typically the first choice for any low-power offline converter. Where isolation is not required, however, this may not be the best approach. Let's say that the end equipment is a smart light switch that users control through a smartphone app. In this case, the user will never be in contact with exposed voltages during operation, so isolation is not required.

For an offline supply, the flyback topology is a reasonable solution, as it has a low bill-of-materials (BOM) count with only a few power-stage components, and the transformer can be designed in such a way to handle a wide input voltage range. But, what if the end application for a design doesn't need isolation? If this is the case, a designer would be tempted to still use a flyback considering that the input is offline. A controller with an integrated field-effect transistor (FET) and primary-side regulation would create a small flyback solution.

Figure 1 shows an example schematic of a nonisolated flyback that uses a UCC28910 flyback switcher with primary-side regulation. While this is a viable option, an offline upside-down buck topology will provide higher efficiency compared to a flyback, with a lower BOM count. In this Power Tip, I will be exploring the benefits of an upside-down buck for a low-power AC/DC conversion.

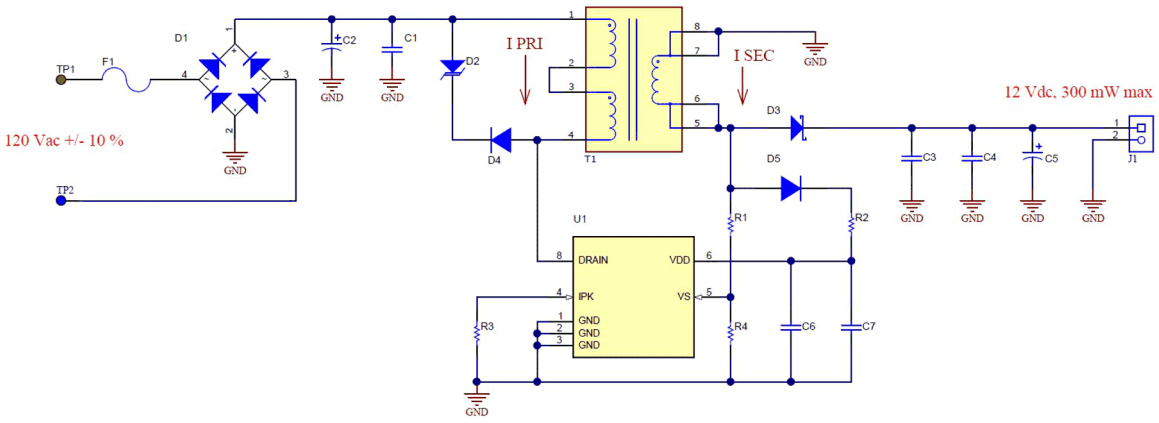

Figure 1. This non-isolated flyback design using the UCC28910 flyback switcher converts AC to DC, but an offline upside-down buck topology can do the job more efficiently.

Figure 1 shows the power stage of an upside-down buck. Like a flyback, there are two switching components, one magnetic (a single power inductor instead of a transformer), and two capacitors. The upside-down buck topology, as the name suggests, is similar to a buck converter. The switches create a switching waveform between the input voltage and ground, which is then filtered out by an inductor-capacitor network. The difference is that the output voltage is regulated as potential below the input voltage. Even though the output is "floating" below the input voltage, it can still power downstream electronics normally.

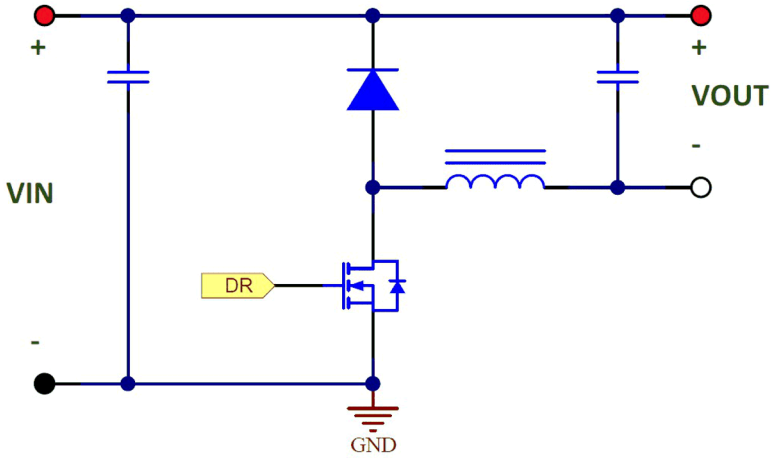

Figure 2. A simplified schematic of an upside-down buck power stage.

Having the FET on the low side means it can be driven directly from a flyback controller. Figure 3 shows an upside-down buck that uses the UCC28910 flyback switcher. A one-to-one coupled inductor functions as the magnetic switching component. The primary winding is acting as the inductor for the power stage. The secondary winding provides timing and output voltage regulation information to the controller's local bias supply (V_{DD}) capacitors.

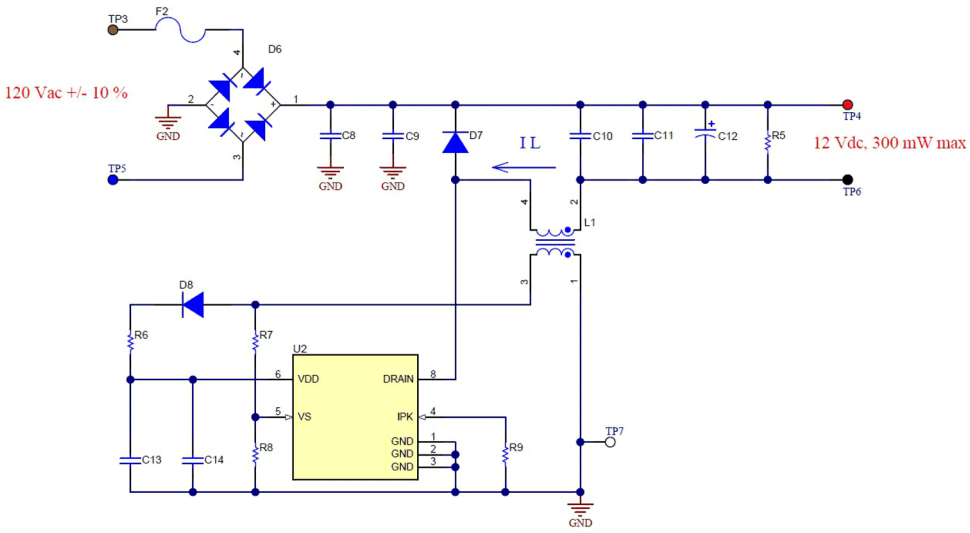

Figure 3. An example upside-down buck design using the UCC28910 flyback switcher.

One drawback of the flyback topology is how energy transfers across the transformer. This topology stores energy in the air gap during the FET's on-time and transfers it to the secondary during the FET's off-time. An actual transformer will have some leakage inductance on the primary side. When energy transfers to the secondary side, what remains is stored in the leakage inductance. This energy is not usable, and requires dissipation using either a Zener diode or a resistor-capacitor network.

In a buck topology, the leakage energy is delivered to the output during the FET's off time through diode D7. This reduces the component count and improves efficiency.

Another difference is the design and conduction losses for each magnetic. Because an upside-down buck only has one winding to transfer power, all of the current for power delivery goes through it, which provides good copper utilization. A flyback does not have as good copper utilization. When the FET is on, current conducts through the primary winding but not in the secondary. When the FET turns off, current flows on the secondary winding and not in the primary. Thus, more energy is stored in the transformer and uses more copper in the flyback design to deliver the same amount of output power.

Figure 4 compares the current waveforms for an inductor of a buck and the primary and secondary windings of a flyback transformer with the same input and output specifications. The buck inductor waveform is in the single blue box on the left, and the primary and secondary windings of the flyback are in the two red boxes on the right.

For each waveform, the conduction loss is calculated as the root-mean-square current squared multiplied by the winding's resistance. Because the buck only has one winding, the total conduction loss in the magnetic is the loss from the one winding. The total conduction loss for the flyback, however, is the sum of the losses from the primary and secondary windings. Additionally, the magnetic will be physically larger in a flyback compared to an upside-down buck design at a similar power level. The energy storage for either component is equal to ½ L × I_{PK}^{2}.

For the waveforms shown in Figure 4, I calculated that the upside-down buck would only need to store one quarter of the power that the flyback would need to store. As a result, an upside-down buck design would have a much smaller footprint compared to an equally powered flyback design.

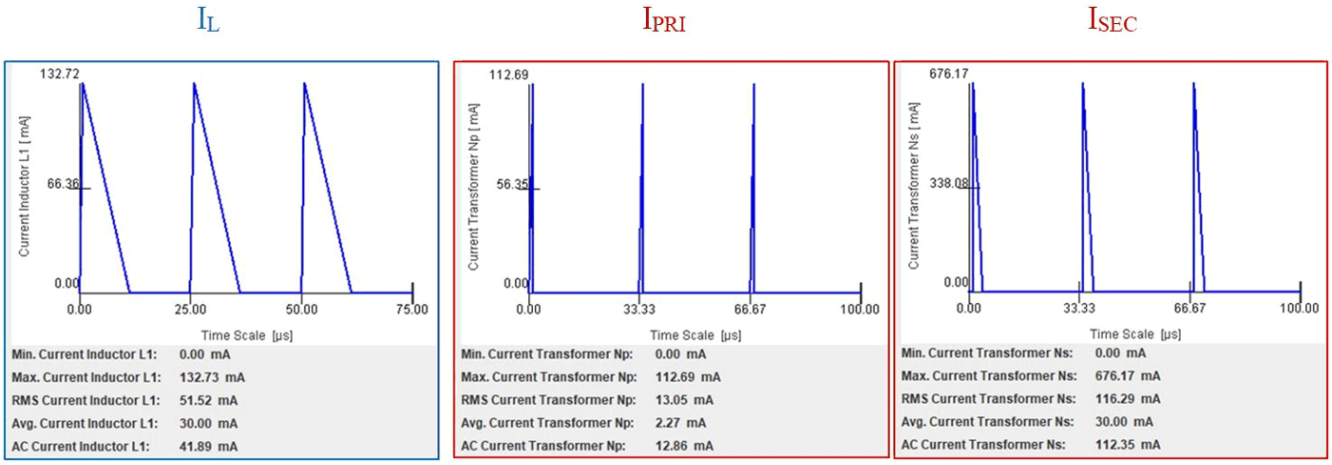

Figure 4. A comparison of current waveforms in buck vs. flyback topologies.

When isolation is not required, the flyback topology isn't always the best solution for a low-power offline application. An upside-down buck can offer higher efficiencies with a lower BOM cost because you can use a potentially smaller transformer/inductor. For a power electronics designer, it is important to consider all possible topology solutions to determine the best fit for the given specifications.

Related articles:

- Power Tips #76: Flyback converter design considerations
- Power Tips #91: How to improve flyback efficiency with a nondissipative clamp
- Creating an isolated power supply creates many challenges
- Isolated power conversion: making the case for secondary-side control
- Build your own oscilloscope probes for power measurements (part 1)
- Build your own oscilloscope probes for power measurements (part 2)

Technical Article

Adding a single capacitor to improve cross-regulation in dual-output flyback power supplies

Brian King

Systems that require multiple output voltages typically employ flyback converters. In these multiple-output flyback converters, maintaining good regulation simultaneously on all output voltages is a big challenge.

Power Tips #78 explored how using synchronous rectifiers can improve cross-regulation between output voltages. The synchronous rectifiers balance the output voltages, but the trade-off is higher root-mean-square (RMS) current in the windings and decreased efficiency at light loads. In this power tip, I'll continue the discussion by looking at a special case that generates positive/negative outputs of the same magnitude. In this situation, proper placement of a single capacitor can improve cross-regulation across all loading conditions.

Figure 1 shows a simplified schematic of a 48-V to ±12-V supply in its normal configuration. To implement the technique proposed here, you must first shuffle the secondary connections around a little, as shown in Figure 1 , by adding capacitor C3 and moving diode D2 from the low side of the secondary winding to the high side. Also, notice that the two transformer secondary windings no longer share a common connection. Other than the added capacitor, C3, Figure 1 is electrically equivalent to Figure 1 .

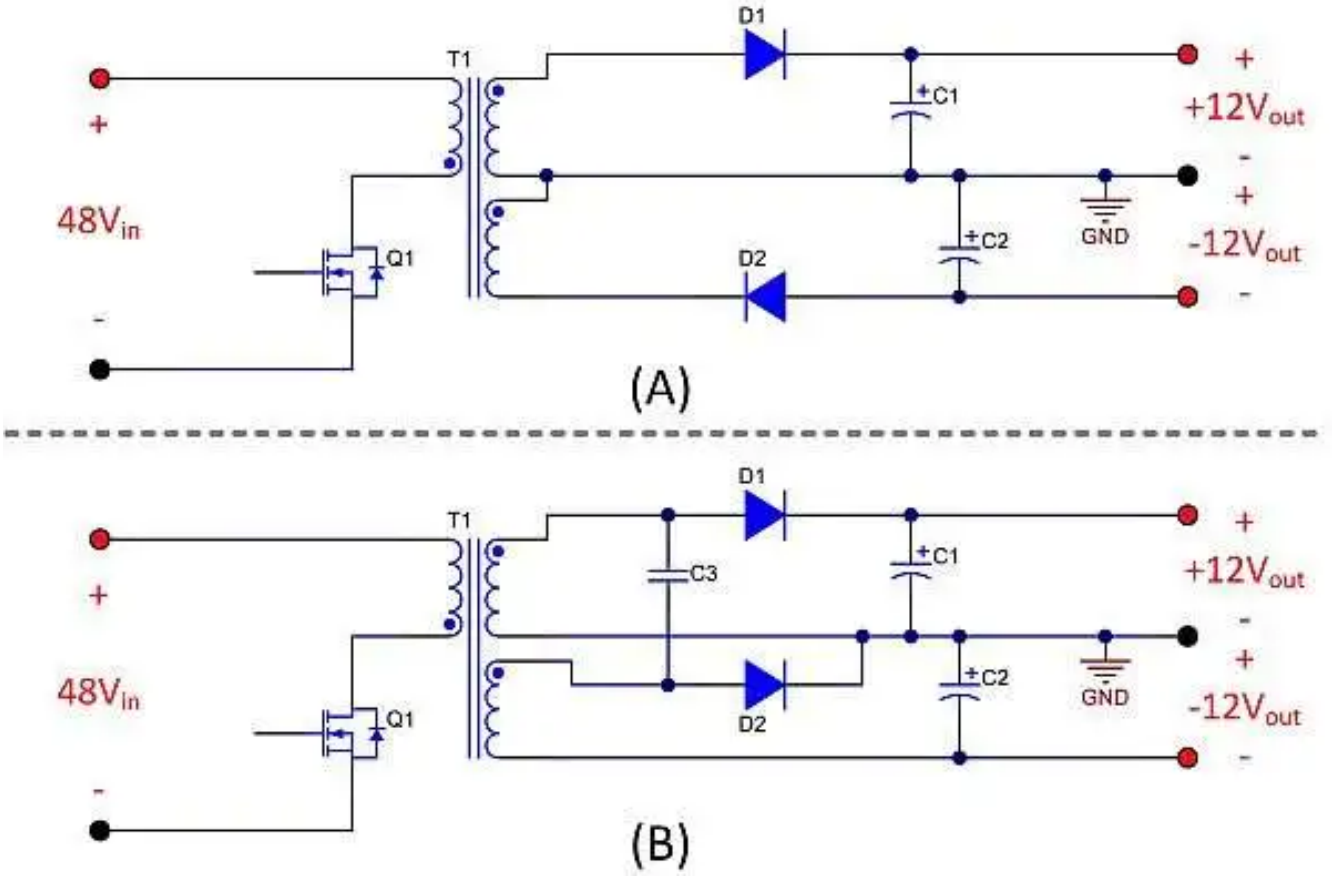

Figure 1. Typical configuration of dual-output flyback supplies (a); reconfiguring and adding a capacitor as shown improves cross-regulation (b).

Figure 2A shows the state of the circuit when Q1 is off and both D1 and D2 are conducting. During this state, the transformer delivers energy to both outputs through the secondary windings. Notice that C3 is connected in parallel with the +12-V output, and thus charges to the same voltage level.

Figure 2B shows the state of the circuit when Q1 is on and both D1 and D2 are reverse-biased and in the off state. During this state, energy is being stored magnetically in the transformer as the primary winding charges from the input voltage. In this state, as long as both secondary windings have the same number of turns, the voltage across C3 is equal to the magnitude of the −12-V output, as described by the equation shown in Figure 2B. As the circuit alternates between these two states, capacitor C3 acts as a charge pump, helping keep the magnitude of both output voltages balanced. This charge-pump effect compensates for voltage imbalances caused by parasitic elements in the circuit. If the two secondary windings have a different number of turns, this technique will not work.

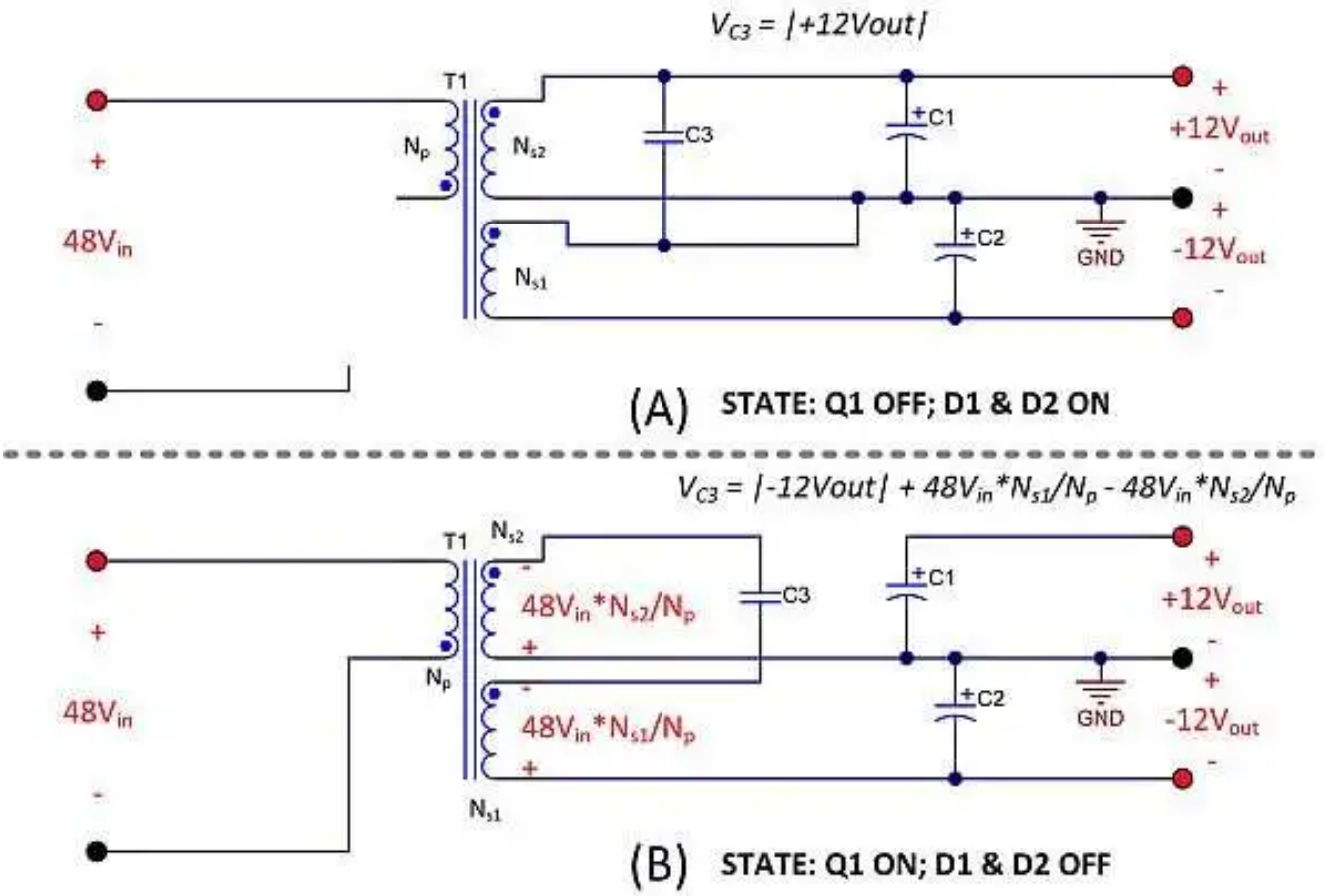

Figure 2. Two states of the circuit: Q1 off, D1 and D2 on (a); Q1 on, D1 and D2 off (b).

Figure 3 shows a simulation schematic modeling the leakage inductances on the primary and secondary windings. As detailed in Power Tips #78, these leakage inductances cause large differences in regulation. The leakage inductance on the primary causes a short duration voltage pedestal to appear on the primary, which couples across to the secondary windings. The leakage inductances on the secondary windings degrade the coupling between the two output voltages.

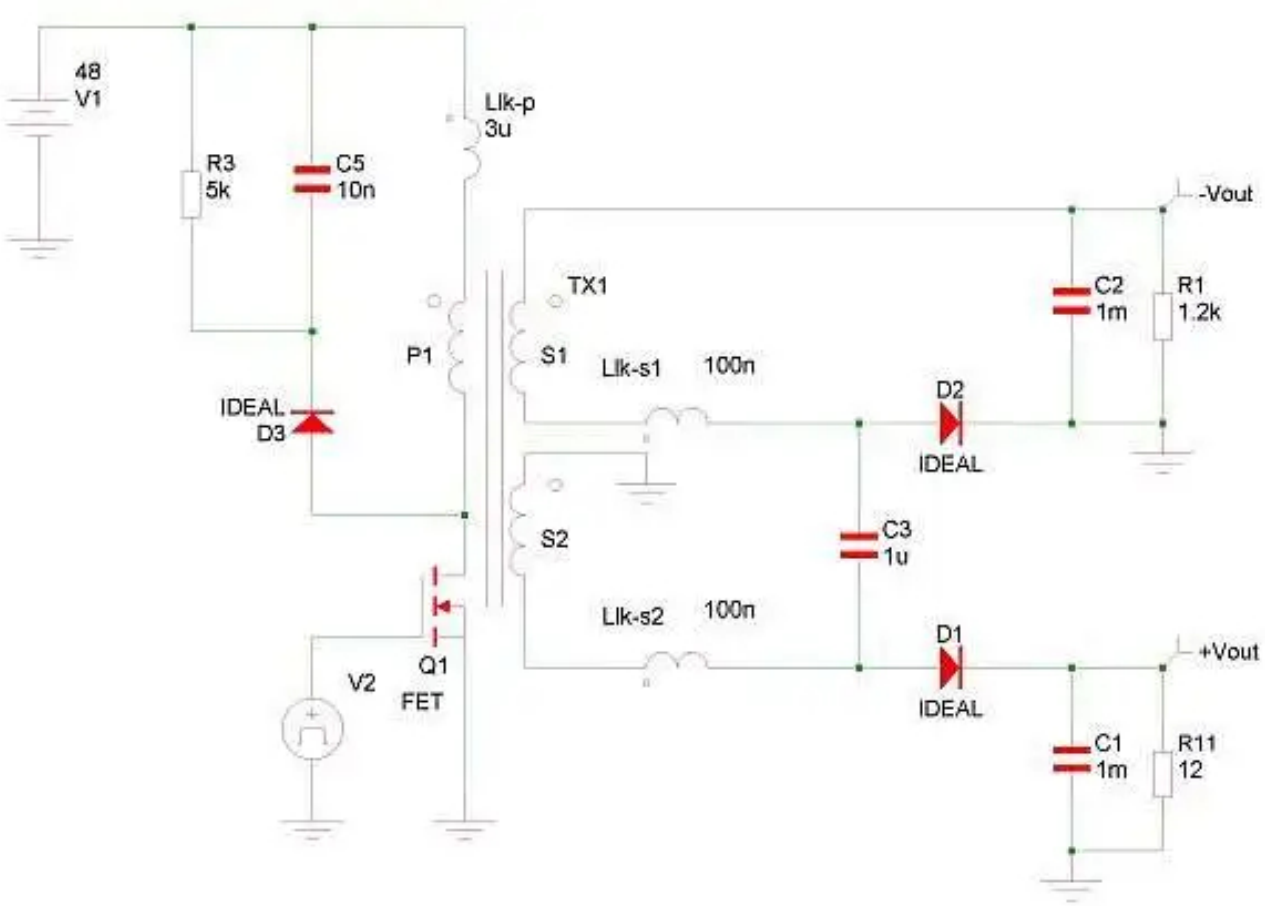

Figure 3. Schematic of a simulation model to investigate the effects of leakage inductance on output-voltage regulation.

Figure 4 shows the voltage and current waveforms in the output diodes when loading the +12-V output with 1 A and the −12-V output with 10 mA. Adding the 1-µF capacitor C3 not only keeps the two outputs well-coupled, but also filters the effects of the voltage pedestal caused by the leakage on the primary winding. Notice the small oscillation on the diode voltage of the more lightly loaded −12-V output. This oscillation is caused by leakage inductances resonating with capacitor C3, and results in a phase shift in the conduction of the −12-V output diode. The current waveform shapes are interesting in that the −12-V current maintains a triangular shape, which subtracts from the +12-V secondary winding current.

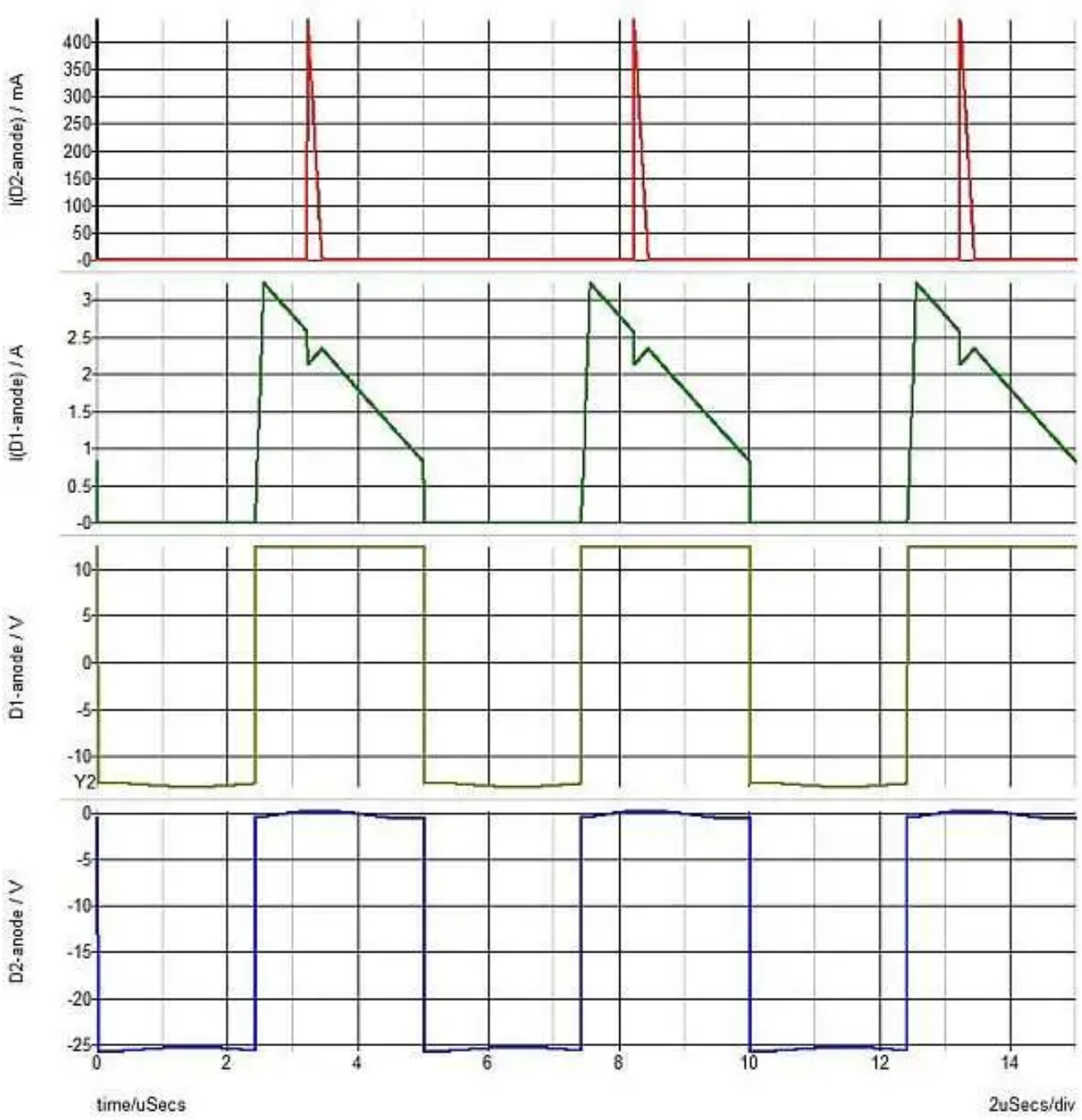

Figure 4. Voltage and current waveforms on the output diodes, with the +12-V output loaded at 1 A and the -12 V loaded at 10 mA.

The graph of Figure 5 shows the regulation impacts of adding the capacitor. Here, simulations are plotted with different loading conditions on the two outputs, both with and without the added capacitor.

Without the capacitor, the −12-V output voltage rises significantly, as the −12-V load decreases toward zero. With the capacitor, both outputs track each other within 3% across the entire load range. These results are similar to those obtained by using synchronous rectifiers, as detailed in Power Tips #78, but without the penalty of increased RMS winding currents, and with very little added cost or complexity.

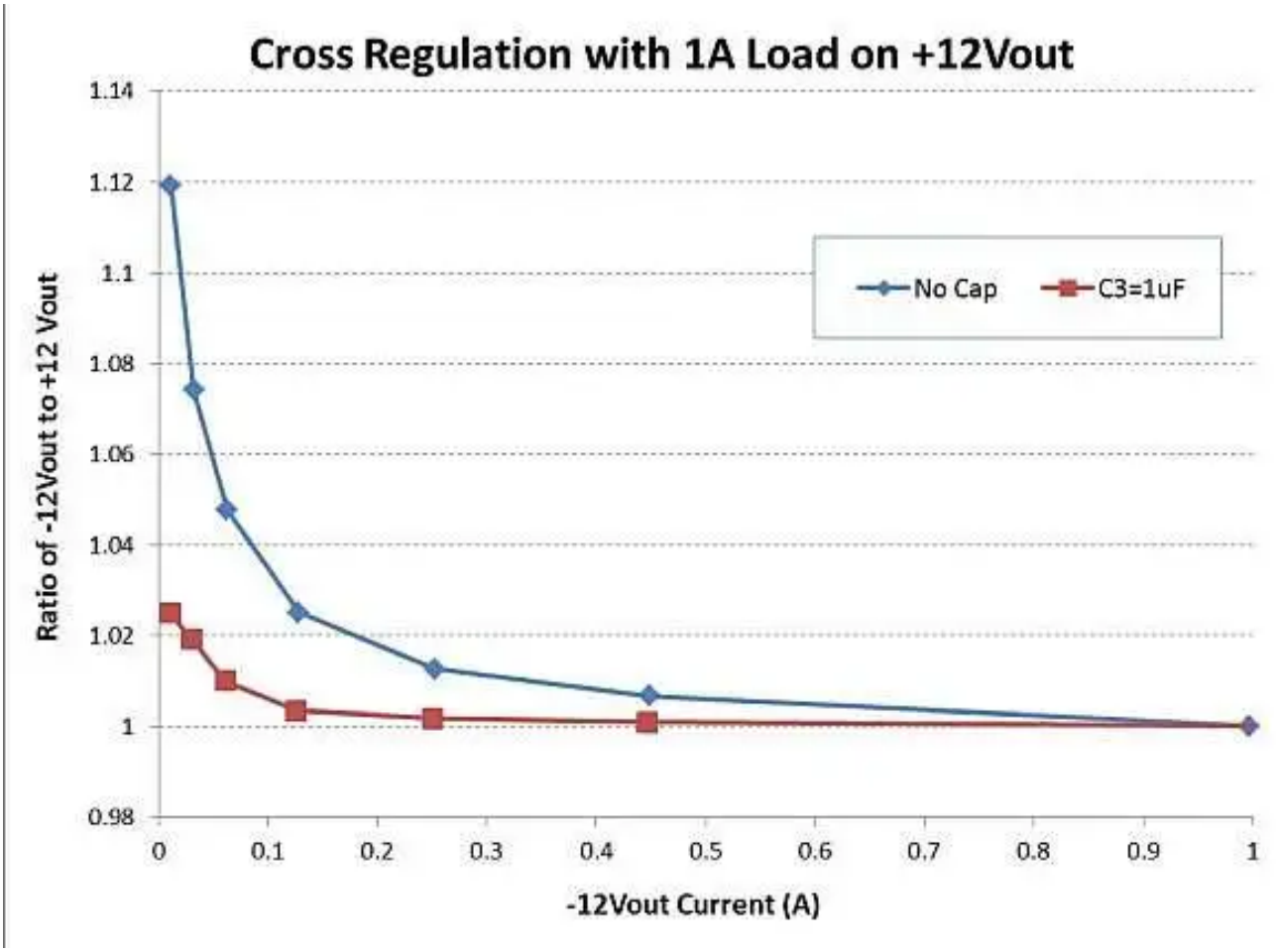

Figure 5. Simulation results show how adding a single capacitor greatly improves cross-regulation.

In conclusion, parasitic leakage inductances conspire to degrade regulation in multiple output power supplies. In supplies with dual positive and negative outputs of equal magnitude, adding a single capacitor can vastly improve the regulation.

In multiple output supplies with different output voltage magnitudes, using synchronous rectifiers is probably the best approach for improving cross-regulation.

The next time you are designing a dual-output power supply, consider implementing this simple technique to improve the performance of your design.

For more Power Tips, check out TI's Power Tips blog series on Power House.

Additional Resources

- Watch the video, "Topology Tutorial: What is a Flyback?"
- Download TI's fly-buck and flyback selector tool to help select the right isolated DC/DC topology based for your specification.

Related articles

- Power Tips #78: Synchronous rectifiers improve cross-regulation in flyback power supplies
- Minimum loads & cross-regulation with multi-output power supplies
- Bringing up a flyback supply for the first time

Technical Article

High-frequency resonant converter design considerations, Part 2

Sheng-Yang Yu

The first installment of this series focused on the key parasitic parameters affecting resonant converter design, along with component selection criteria and transformer design. This installment focuses on resonant converter synchronous rectifier (SR) design considerations.

The operational states in a resonant converter can be much more complex than in a pulse-width modulation converter. Taking the inductor-inductor-capacitor-series resonant converter (LLC-SRC) in Figure 1 as an example, there are four common states (Figure 2) in a regular LLC-SRC design with given load conditions and relative positions of switching frequency (f_{sw}) and series resonant frequency (f_r). When f_{sw} r, the rectifier diode current goes to zero before an active switch (Q_1 or Q_2) turns off. Therefore, when applying a metal-oxide semiconductor field-effect transistor (MOSFET) as a rectifier (that is, an SR), the SR must be turned off with less than a 50% duty cycle to avoid rectifier current backflow. Otherwise, the converter efficiency will be harmed by excessive circulating current.

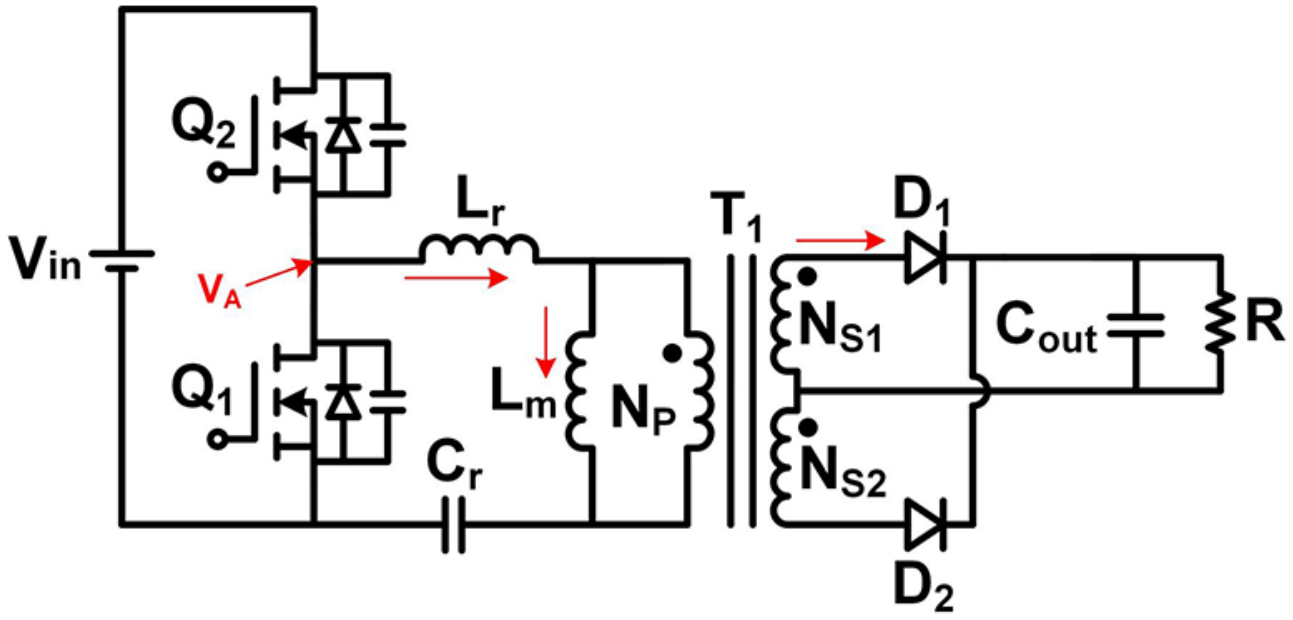

Figure 1. An inductor-capacitor series resonant converter (LLC-SRC) provides soft-switching features that allow high-frequency operation.

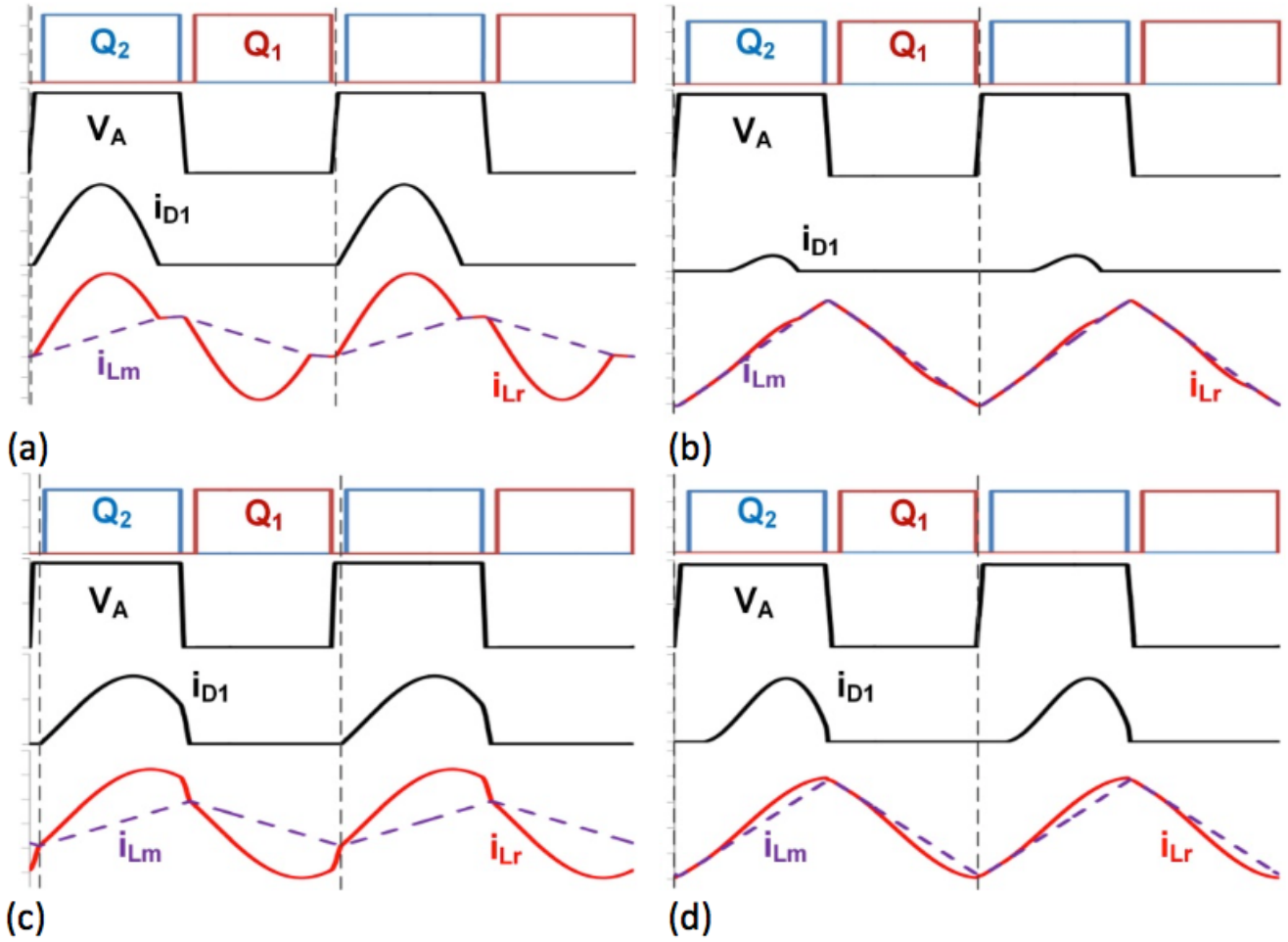

Figure 2. Operational states of an LLC-SRC under heavy load and f_{sw}r (a), light load and f_{sw} r (b), heavy load and f_{sw} >f_r (c), and light load and f_{sw} >f_r (d) show the need of current sensing to avoid reverse current flow on the output rectifier if SR is applied.

The rectifier current conduction time is actually 0.5/f_r at a heavy load when f_{sw} r . So it is possible to limit the SR conduction time to be slightly less than 0.5/f_r at a heavy load when f_{sw} r and disable the SR at a lighter load [1]. This open-loop SR control method won't be able to optimize converter efficiency, however.

A more reliable SR control method is through MOSFET drain-to-source voltage (V_{DS}) sensing [2] (Figure 3). Basically, this SR control method compares the MOSFET V_{DS} with two different voltage thresholds to turn the MOSFET on and off. Some newer V_{DS} sensing SR controllers like the UCC24624 from Texas Instruments even have a third voltage threshold to activate a proportional gate driver for fast SR turn off with minimal delay.

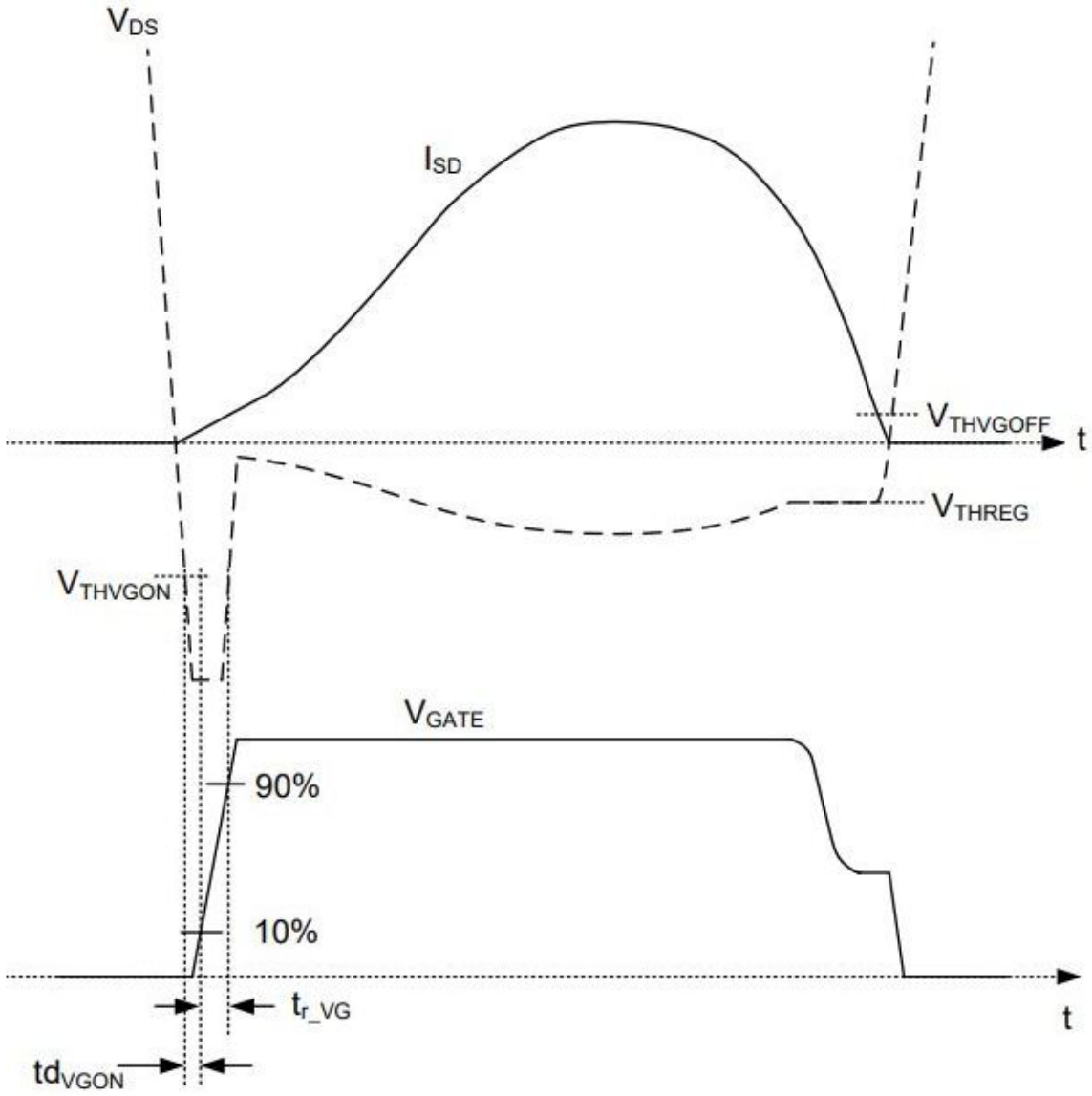

Figure 3. V_{DS} sensing SR turns SR on and off at different V_{DS} voltage levels.

It is notable that the voltage thresholds are in the millivolt levels; high-accurate sensing circuitry is required. Therefore, the V_{DS} sensing method is generally realized by using integrated circuits, which have a V_{DS} level (less than 200V in general) and f_{sw} limitations (less than 400kHz in general). Due to the limitations the V_{DS} sensing SR control method have, you will need a different SR control method to optimize SR conduction for high-voltage and high-frequency resonant converters.

Using a Rogowski coil [3] followed by integrator and comparators is an alternative way to control a high-frequency resonant converter SR. Figure 4 is a block diagram illustrating SR control with a Rogowski coil on a capacitor-inductor-inductor-inductor-capacitor series resonant dual active bridge converter (CLLLC-SRes-DAB) [4]. An air core coil with windings – a Rogowski coil – is placed on the transformer winding for current sensing. When a time-varying current flows through the coil, the current-generated magnetic flux induces voltage on the coil windings. The induced voltage will have a 90-degree phase difference when compared to the original time-varying current.

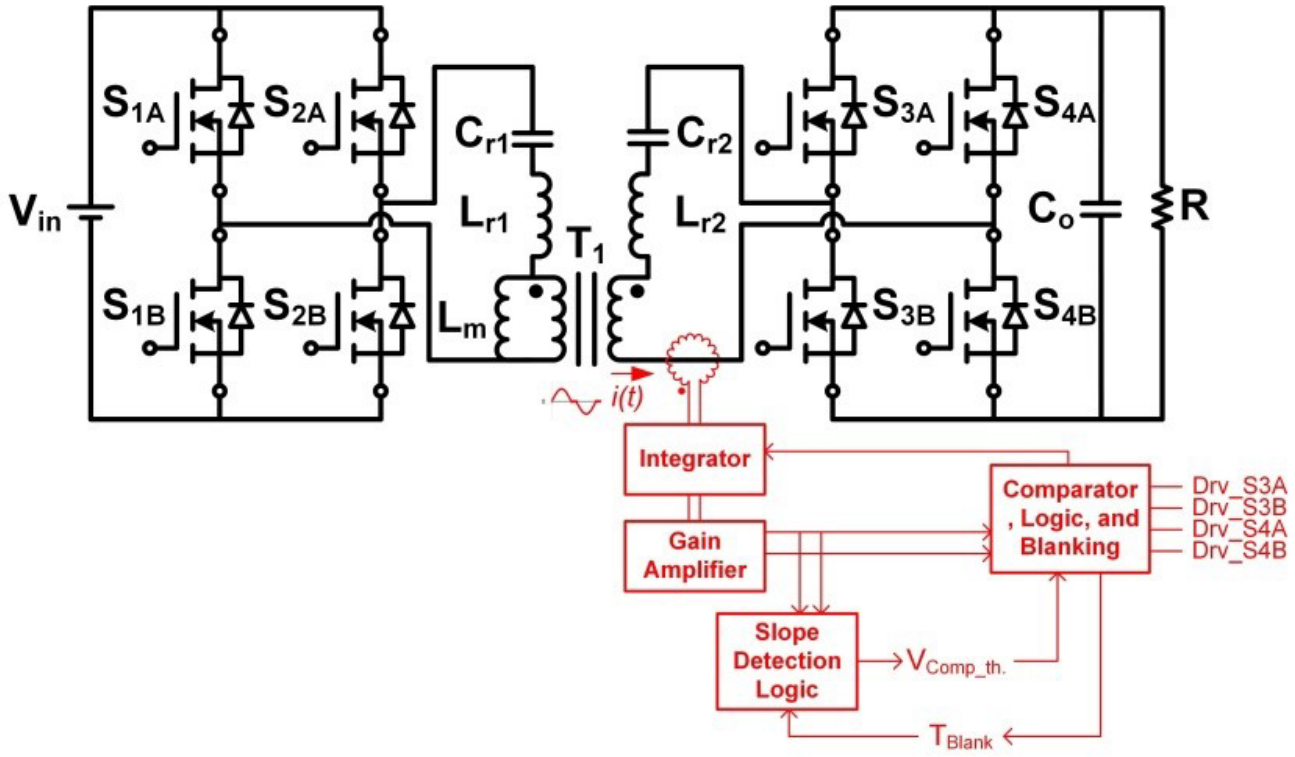

Figure 4. Rogowski coil SR control enables accurate high-frequency SR sensing and control in a CLLLC-SRes-DAB converter.

Adding an integrator after the Rogowski coil can generate a voltage that is in phase or even leading the original time-varying current. Thus, it is possible to set the zero voltage crossing of the integrator output to be a little bit earlier than the time-varying current zero current crossing to accommodate possible propagation and control delay. The amplified integrator output signal is then compared with a given comparator threshold to generate a SR driving signal with a nearly optimized SR conduction time. Additional slope detection logic inserted in the control circuit further optimizes SR conduction times over different load conditions. Because a Rogowski coil senses current by magnetic flux, there is no voltage-level limitation. Also, a Rogowski coil uses air core instead of magnetic core material, so its bandwidth is very high without saturation limit; thus, there are no frequency limitation concerns even on megahertz level resonant converters unlike the V_{DS} sensing SR control method.

Figure 5 illustrates the method proposed here. Defining the time-varying current in Figure 5 to be *i(t)* and assuming that the Rogowski coil is placed vertically on the transformer winding, you can use Equation 1 to calculate the Rogowski coil winding output voltage as:

$$V_{1\_0}(t) = \frac{-AN\,\mu_0}{l}\frac{di\,(t)}{dt} \tag{1}$$

where *A* is the cross-section area of each turn on the Rogowski coil (assuming that the turns on the Rogowski coil all have the same area of the cross section), *N* is the number of turns on the Rogowski coil, *l* is the circumference of the Rogowski coil ring, and $\mu_0 = 4\pi \cdot 10^{-7}$ H/m is the permeability constant.

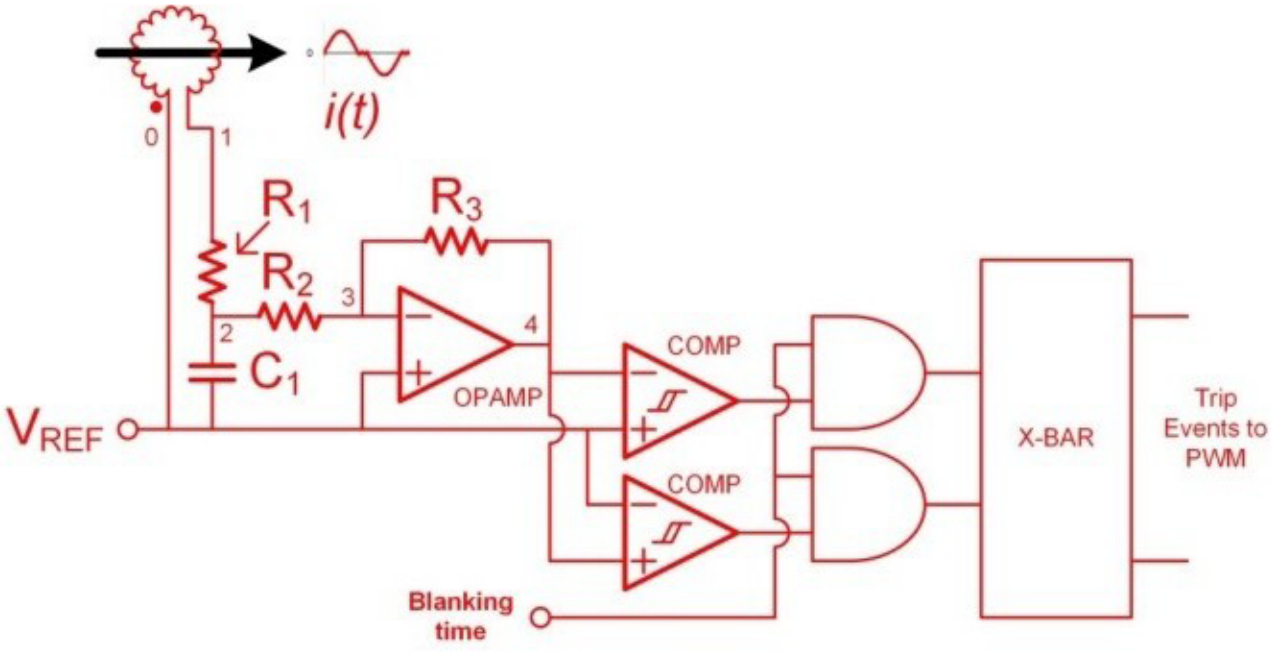

Figure 5. Passive integrator allows the Rogowski coil SR control circuit to predict the zero current crossing timing.

Assuming the use of an ideal operational amplifier used in the proposed sensing circuit, Equation 2 expresses the voltage relationship between the Rogowski coil output v_{1_0} and the passive integrator output v_{2_0}:

$$\frac{dv_{2\_0}(t)}{dt} + \left(\frac{1}{R_1C_1} + \frac{1}{R_2C_1}\right)V_{2\_0}(t) = \frac{V_{1\_0}(t)}{R_1C_1} \tag{2}$$

It's possible to solve the differential equation in Equation 2 in the form of Equation 3

$$V_{2\_0}(t) = \frac{1}{I}\int I\frac{V_{1\_0}(t)}{R_1C_1}dt + \frac{a_0}{I} \tag{3}$$

where a_0 is a constant, expressed by Equation 4.

$$I = e^{\left(\frac{1}{R_1C_1} + \frac{1}{R_2C_1}\right)t + constant} \tag{4}$$

To more easily understand how to adjust the phase difference with the passive integrator and amplifier, assume that the time-varying current is purely sinusoidal, which will make both the Rogowski coil output voltage and the integrator output purely sinusoidal. In other words, solving Equation 1 and Equation 2 to get the solution of *i(t)* with the assumption of $v_{2\_0}(t) = a_1 \sin(\omega t)$, Equation 2 can be rewritten as Equation 5:

$$i\left(t\right) = \frac{a_1 l}{AN\mu_0}\sin\left(\omega t + \emptyset + \frac{\pi}{2}\right) \tag{5}$$

where Equation 6

$$\emptyset = \tan^{-1}\left(\frac{a_1\omega}{a_2}\right) = \tan^{-1}\left[\frac{\omega}{\left(\frac{1}{R_1C_1} + \frac{1}{R_2C_1}\right)}\right] \tag{6}$$

Flipping the pinouts of the Rogowski coil, the time-varying current becomes Equation 7:

$$i(t) = \frac{a_1 l}{AN\mu_0} \sin\left(\omega t + \emptyset - \frac{\pi}{2}\right) \quad (7)$$

When making Φ = −π/2 for Equation 3 and Φ = π/2 for Equation 4 by varying the values of R_1 , R_2 , C_1 and the f_{sw} ($\omega = 2\pi f_{sw}$) with the right connection polarity between the Rogowski coil output and integrator input, the integrator output $v_{2\_0}(t)$ can be in phase with the SR current *i(t)*. Moreover, in practical applications, you can set the integrator waveform to lead the SR current. So with the response time and propagation delay on the controller and driver, respectively, the SR turn off timing can still manage to be at the zero current crossing point.

Figure 6 shows the winding current measurement and gain amplifier output voltage of the sensing circuit. As you can see, programming zero voltage crossing to turn off earlier than the actual sensing current accommodates propagation and control delays.

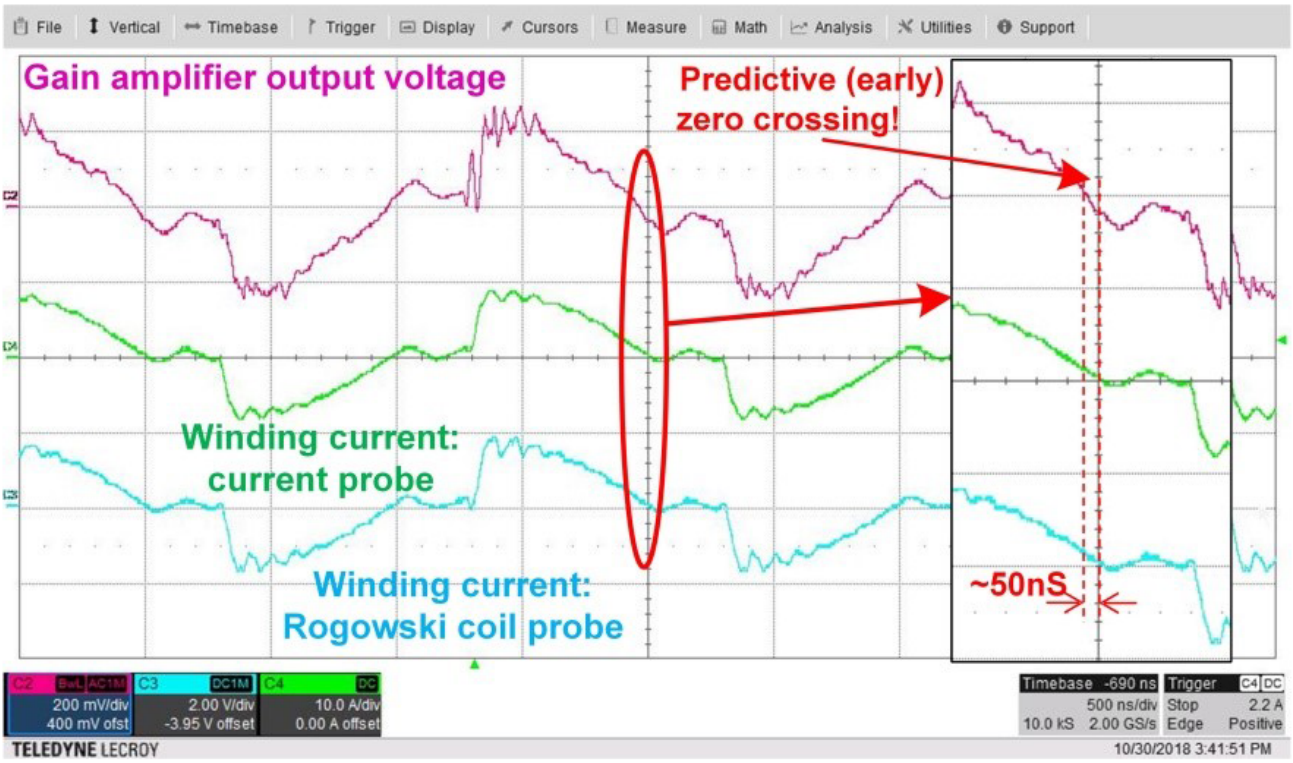

Figure 6. This SR current measurement comparison shows the predictive SR sensing by having zero current crossing at integrator output earlier than actual zero current crossing.

Figure 7 shows perfect SR turn-off timing when the switching frequencies are below the series resonant frequency.

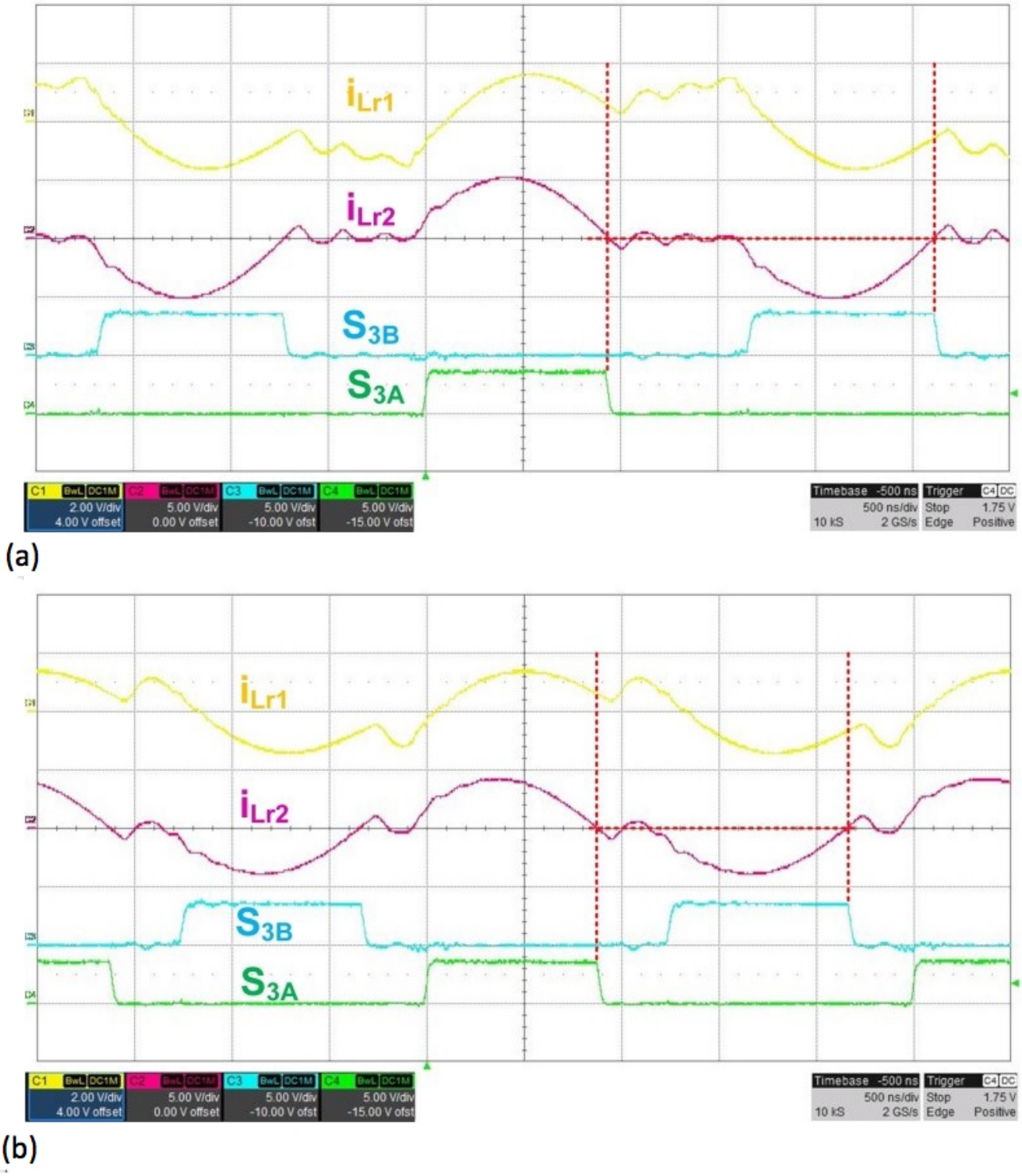

Figure 7. SRs are turning off at perfect zero current crossing at 300 kHz (a) and 400 kHz (b).

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1. J. Wang and B. Lu, “Open loop synchronous rectifier driver for LLC resonant converter,” in Proc. APEC, 2013, pp. 2048-2051.
2. UCC24624 dual-channel synchronous rectifier controller for LLC resonant converters, Texas Instruments
3. M.H. Samimi, A. Mahari, M.A. Farahnakian and H. Mohseni, “The Rogowski Coil Principles and Applications: A Review,” IEEE Sensors Journal, vol. 15, pp. 651-658, 2015.
4. B. Zhao, Q. Song, W. Liu and Y. Sun, “Overview of Dual-Active-Bridge Isolated Bidirectional DC-DC Converter for High-Frequency-Link Power-Conversion System,” IEEE Transactions on Power Electronics, vol. 29, pp. 4091-4106, 2014.

Related articles

- Power Tips #89: High-frequency resonant converter design considerations, Part 1
- Using quasi-resonant and resonant converters
- Measure small impedances with Rogowski current probes
- High efficiency resonant mode implementation using digital control
- Power Tips #84: Think outside the LLC series resonant converter box

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