Dynamic Limiter

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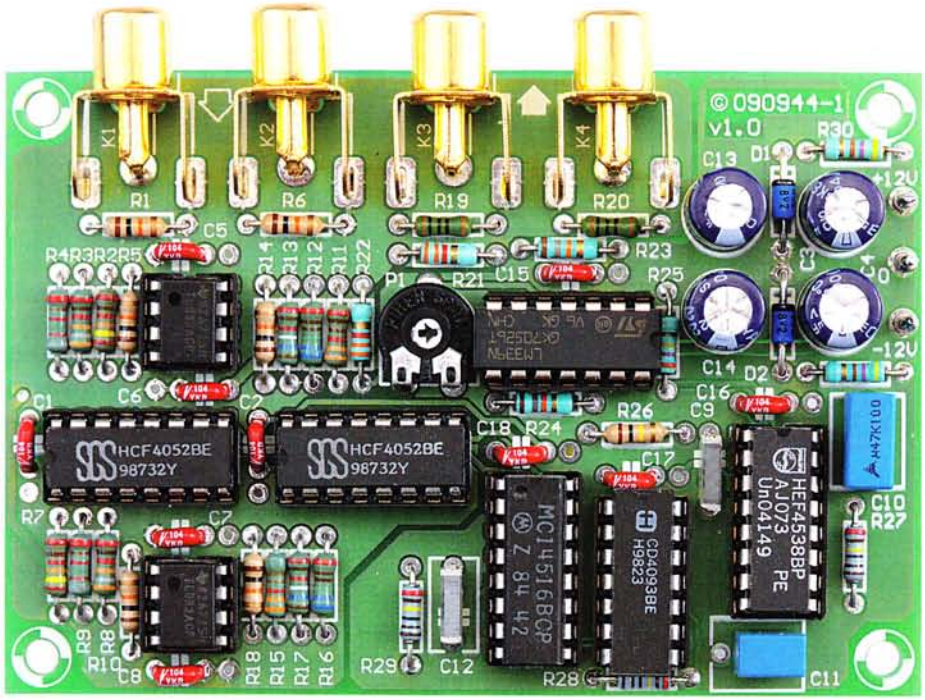
This circuit is a revised version of the Audio Limiter published in the 2002 Summer Circuits edition, which is intended to limit the (possibly excessive) dynamic range of the audio signal from a TV set or DVD player (for example). The original circuit is based on attenuating an excessively strong source signal. Here we take the opposite approach of amplifying the quieter passages. To minimise the typical 'breathing' effect of compressors, the control range is limited to only 24 dB. The gain is adjusted in discrete (non-audible) steps, which avoids non-linearity and thus avoids distortion.



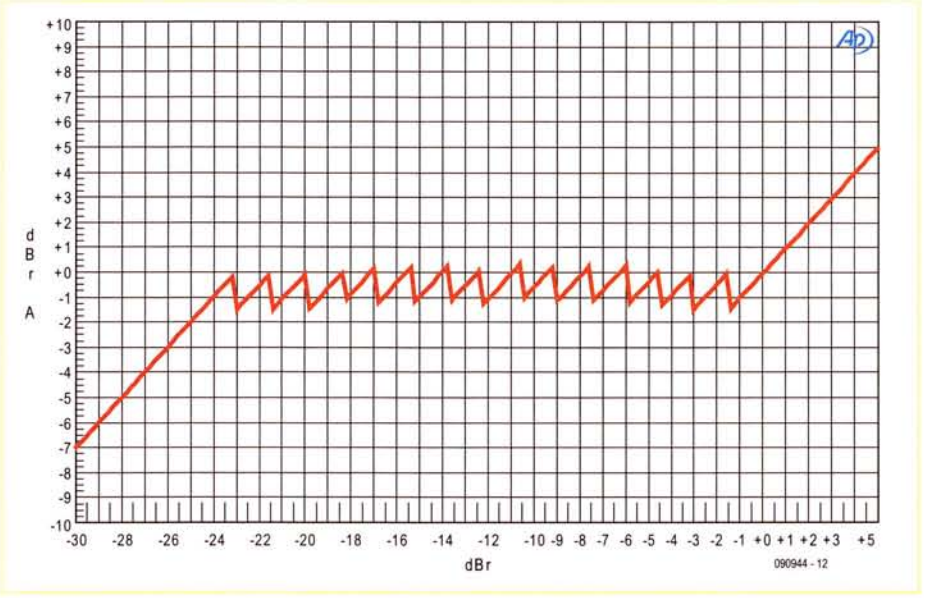
With the component values shown on the schematic diagram, the circuit can boost the gain in 15 steps of 1.6 dB each, yielding 16 levels from 0 to 24 dB. The voltage divider used in the original circuit has been replaced here by negative feedback circuitry using two non-inverting amplifiers. This reduces the number of resistors and allows smaller multiplexers to be used — in this case consisting of two halves of a 4052 IC per channel (the 4052 is a dual 1-of-4 analogue multiplexer/demultiplexer).

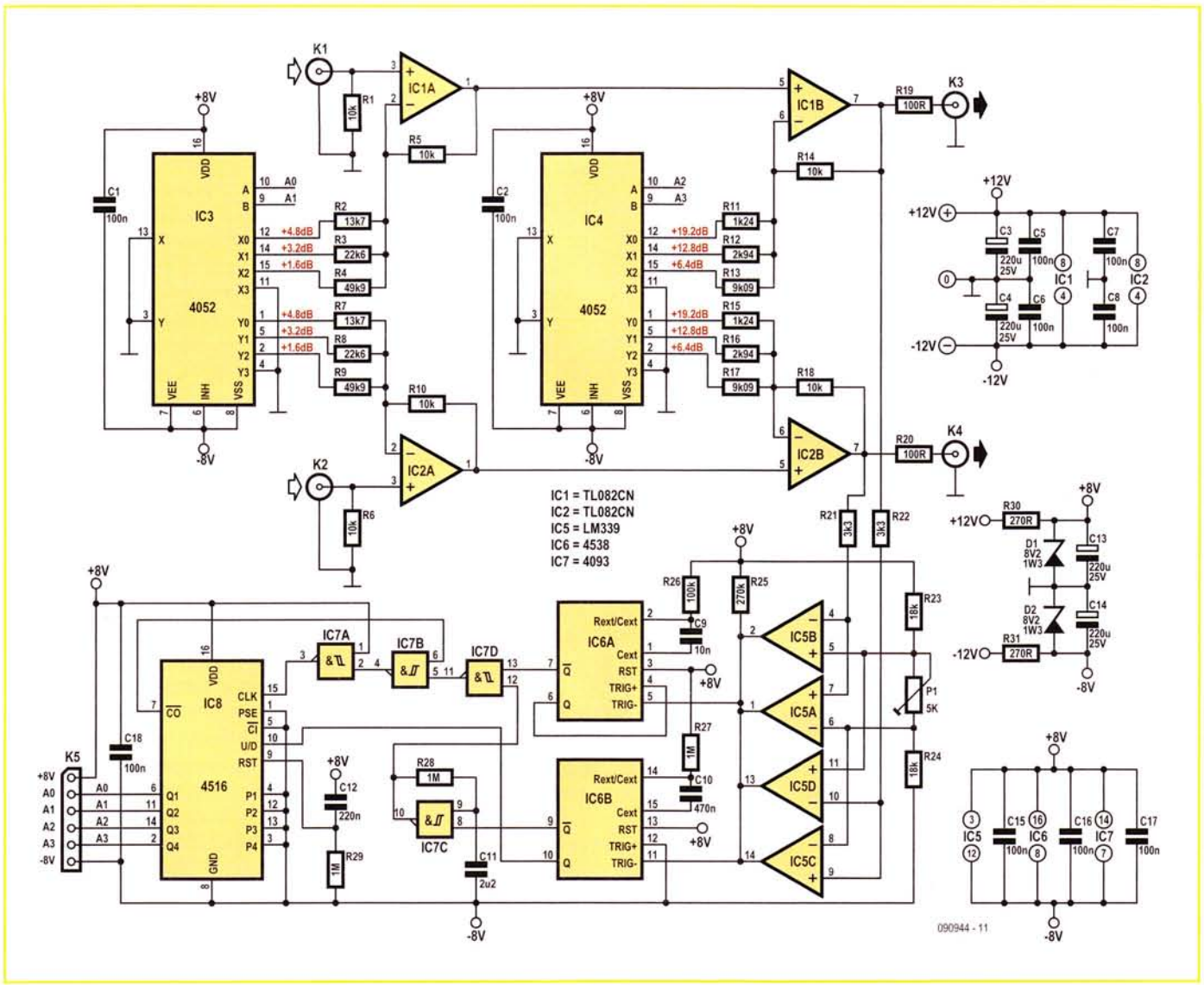
The entire control logic is the same as before. Although there are two stages per channel, fewer resistors are necessary than with the original design. To allow the overall gain to be controlled in equal steps, the individual amplifiers (IC1A/IC3 and IC1B/IC4) have different step sizes. The gain steps of the first stage are relatively small (0, 1.6, 3.2 and 4.8 dB), while the gain steps of the second stage are relatively large (0, 6.4, 12.8 and 19.2 dB). The total gain can thus be controlled over a range of 0 to 24 dB in 16 equal steps. The individual resistor values are easy to calculate with this approach: $(10\ k\Omega)/(10^{A/20} - 1)$, where A is the desired gain and 10 kΩ is the value of R5, R10, R14 or R18. Other gain ranges can also be implemented in this manner (see **table**), but you should bear in mind that steps larger than 1.6 dB may be audible.

The control circuitry is largely made up of simple discrete logic. The multiplexers are driven by an up/down counter (IC8). Window comparators are used to determine the signal level at the output. They are built around two comparators of an LM399 (quad comparator) for each channel. The same reference voltage (across P1), at approximately 1 V, can be used for both channels. The reference voltage can be modified by changing the value of P1 — for instance, 10 kΩ yields around 1.7 V. The con-

Table. Alternative control ranges (R5 = R10 = R14 = R18 = 10 k)

	15 dB			20 dB		
	Theoretical	E24	E96	Theoretical	E24	E96
R2 & R7	24.24 kΩ	24 kΩ	24.3 kΩ	17.10 kΩ	18 kΩ	16.9 kΩ
R3 & R8	38.62 kΩ	39 kΩ	38.3 kΩ	27.83 kΩ	27 kΩ	28.0 kΩ
R4 & R9	81.95 kΩ	82 kΩ	82.5 kΩ	60.27 kΩ	62 kΩ	60.4 kΩ
R11 & R15	3.354 kΩ	3kΩ3	3.32 kΩ	1.883 kΩ	1.8 kΩ	1.87 kΩ
R12 & R16	6.614 kΩ	6kΩ8	6.65 kΩ	4.142 kΩ	4.3 kΩ	4.12 kΩ
R13 & R17	17.10 kΩ	18 kΩ	16.9 kΩ	11.80 kΩ	12 kΩ	11.8 kΩ





trol circuit responds to the peak level of the output signal. As long as the output signal level is lower than the reference level, oscillator IC7c is enabled by monostable multivibrator IC6b. This causes IC8 to count down slowly (pen 10 of IC6 is low) until the lowest count is reached. The counter is then blocked by IC7b, and the gain is set to the maximum (the X0 outputs of IC3 and IC4 are at ground level). IC6b is triggered when the window comparators generate pulses. The outputs of IC6b remain asserted as long as this occurs (the 4528 is retriggerable), and oscillator IC7c is blocked. IC6a is now triggered by the comparators. The Q output of IC6a is connected to the positive trigger input to prevent retriggering of IC6a. In this situation the counter is clocked by pulses from IC6a (pin 7).

The pulse width is set to 1 ms to prevent the multiplexers from going a few steps too far at high frequencies. If you find the recovery time too long, you can make it shorter by reducing the value of R26. The time delay provided by IC6b ensures that the circuit does not start amplifying the audio signal right away, but instead waits for half a second. This gives the circuit a calmer control characteristic.

The circuit is designed for a minimum gain of 1. Signals larger than the set reference level are passed through unchanged. As the quieter passages in the audio signal are amplified, you can set the volume control of your sound system to match the loudest sound level. A circuit that simplifies the optimal adjustment of P1 is described elsewhere in this Summer Circuits edition.

The logic circuitry operates from symmetrical 8-V supply voltages. They are derived from the symmetrical 12-V supply rails with the aid of two resistors and two Zener diodes. The values of these components as shown on the schematic diagram are dimensioned for the external indicator circuit, which can be connected to K5. The current consumption is approximately 20 mA. If you don't use the indicator, the current consumption can be reduced by 5 mA by increasing the values of R30 and R31 to 470 Ω. The distortion is very low – only 0.001% at 1 kHz with 500 mV input and output levels.

The measured characteristic curve shows the behaviour of the circuit. The X axis represents the input signal, while the Y axis represents the output signal. Here 0 dB corresponds to the reference level. The 24 steps of controlled gain adjustment as the input signal level increases are clearly visible here.

A PCB layout for the circuit and the accompanying components list may be downloaded from the Elektor website [1].

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[1] www.elektor.com/090944